PCBheaven

The BJT Transistor Theory

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Revision A

Preface

The purpose of this book is to help the reader to understand how transistors work and how to design a simple transistor circuit. It is addressed to amateur circuit designer with little or no previous knowledge on semiconductors. Consider the contents of this book as the first mile of a long journey into transistor circuits.

The book exclusively covers practical topics that the amateur circuit designer will find easy to follow, but the professional or the theoretical researcher may find poor. For the sake of ease the mathematical formulas are kept as simple as possible and as less as possible. Nevertheless, since no circuit analysis can be achieved without mathematics, the reader may have to go through some -hopefully- simple and short calculations.

The first chapter swiftly explains how a transistor is made and how the electrons flow, as well as there is a quick reference on the hybrid parameters of a transistor. The second chapter is about the different transistor connections and the different biasing methods. In the third chapter you will learn how to draw the DC load line and how to set the quiescence point Q. Going on to the fifth chapter we discuss about the operation of the transistor in AC. Here you will learn to draw the AC load line, extract the T and Π equivalent circuits and set the optimum quiescence point Q for maximum undistorted amplification. Finally in the fifth chapter you will learn how to calculate the power dissipation on the transistor and how to calculate the efficiency of an amplifier.

CHAPTER 1

How BJT Transistors Work

This chapter explains how the transistor works, as well as the hybrid parameters of a transistor. Since this book is intended to be used as a circuit design aid and not for theoretical research, we will not go through many details.

1 How BJT transistors Work

1.1 Inside a Transistor

A **BJT (Bipolar Junction Transistor)** has inside two similar semiconductive materials, and between them there is a third semiconductive material of different type. These semiconductor materials can either be a P type (positive) with an excess of holes, or a N type (negative) with an excess of electrons. So if the two similar materials are P and the middle one is N, then we have a P-N-P or PNP transistor. Similarly, if the two materials are N and the middle one is P, then we have a N-P-N material or NPN.

Each transistor has 3 leads which we call base, collector and emitter, and we use the symbols b, c and e respectively. Each lead is connected to one of the 3 materials inside, with the base being connected to the middle one. The symbol of the transistor has an arrow on the emitter. If the transistor is a PNP, then the arrow points to the base of the transistor, otherwise it points to the output. You can always remember that **the arrow points at the N material**. These are the symbols:

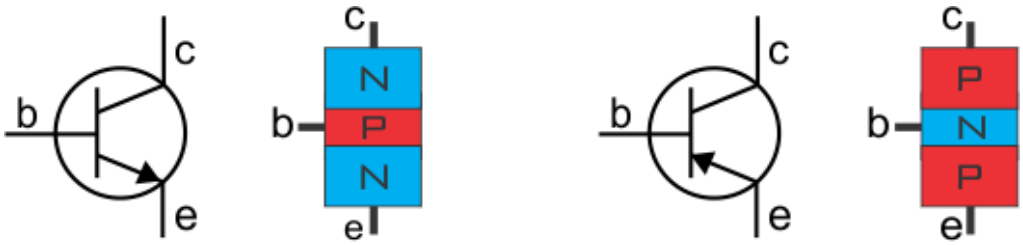

Fig. 1.1 – The NPN (left) and PNP (right) transistor symbols. You can remember the symbols by remembering that the emitter arrow always points at the "N" layer

1.2 Transistor Operation

1.2.1 Understanding the Transistor through a Hydraulic Model

We will now explain the operation for the transistor, using an NPN type. The same operation applies for the PNP transistors as well, but with currents and voltage source polarities reversed. Since the purpose of this book is not to go deeply into the physics of the transistor operation, there will be no references to the movement of electrons.

You can imagine the transistor as an electronic proportional switch. This switch has an input, an output and a control. Current flows through the input to the output. The amount of this current is controlled by the current through the control. Also, the current that flows through the transistor (input-output) is many times bigger than the current through the control. These two previous statements roughly describe the transistor operation.

Let's see an example of such a switch, but instead of using a transistor, we will use a hydraulic valve model. This valve will simulate an NPN transistor.

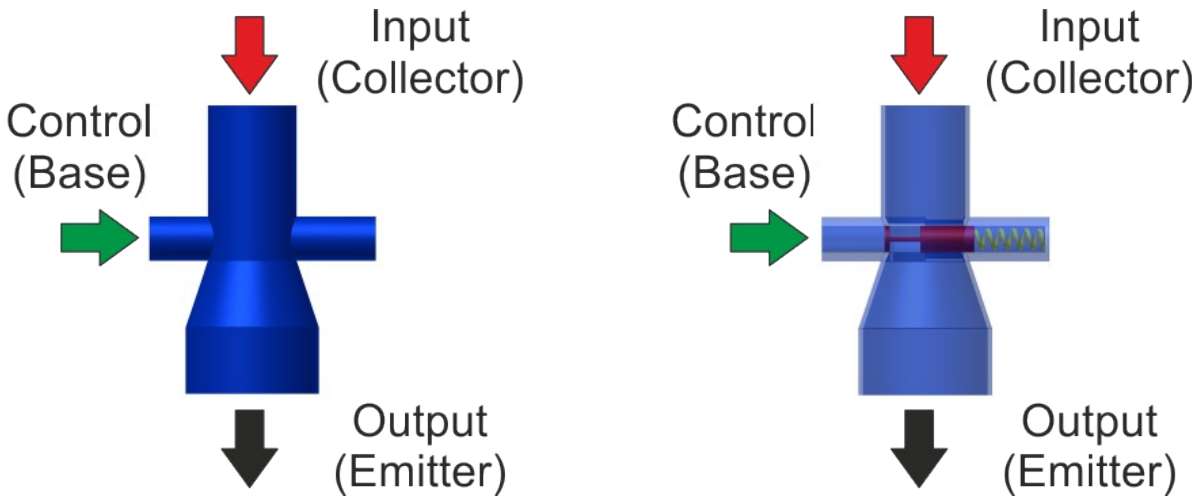

Fig. 1.2 – A hydraulic valve can be used to simulate the transistor operation. The figure on the right is the same valve with its shell semi-transparent for the piston and the tension spring to appear.

Figure 1.2 is the hydraulic valve which simulates the transistor operation. The left image shows the valve shell while the image on right side has this shell semi-transparent. The valve piston (red) and the tension spring (yellow) are visible. In figure 1.3 is a close up section of the valve. Now the operation can be easily described. But first lets declare the two main figures to maintain consistency. The electric voltage is represented as water pressure. Higher water pressure is used to demonstrate higher electric voltage. Similarly, water flow is used to represent the electric current. Faster water flow is used to demonstrate higher electric current.

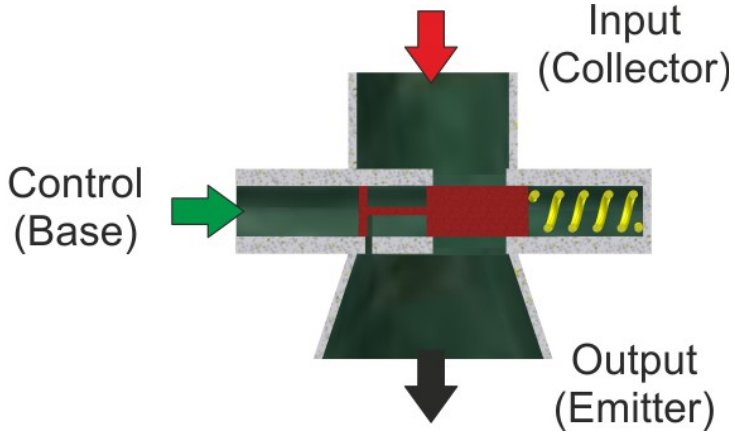

Fig. 1.3 A close-up section of he hydraulic valve

The main water supply is connected at the input of the valve. The piston blocks the way to the output, so no water flows through the valve (Fig. 1.4). Then we begin to increase the pressure (voltage) onto the piston by supplying low pressure water. The piston will begin to move and the spring will contract to compensate this force. Nevertheless, no water will flow (current) through the control neither through the input as long as the control pressure is kept low (Fig. 1.5). This specific threshold is called **Base-Emitter voltage V_{BE}** and depends on the material that the transistor is made of. **Germanium** (Ge) was originally used to make transistors, and later **Silicon** (Si) was used. For Germanium, this voltage is around **0.3 volts** (0.27 @ 25^{o}C), and for Silicon this voltage is

around **0.7 volts** (0.71 @ 25°C). Obviously in this hydraulic model this threshold depends on the mechanical characteristics of the tension spring. Further increasing the control pressure will cause the piston to move even more, revealing the small passage from the control to the output. This will cause a small amount of water to flow through this passage (Fig. 1.6). This is the **Base Current I_B**. This current is usually in the scale of microamperes or a few miliamperes. This current depends on the **Base Voltage (V_B)**, and the **internal resistance of the Base-Emitter contact r'_e**. In our hydraulic model this internal resistance is the small slot through which the water flows from the control (Base) to the output (Emitter).

Meanwhile the passage between the Input and the Output opens and water flows through the transistor. This water flow is the **Collector Current I_C** and depends on the water pressure at the input and the width of the passage between the input and the output. This water pressure is the **Collector Voltage V_{CC}**. It is obvious that the water from both the control and the input (Base Current and Collector Current) appear at the output. This is the **Emitter Current I_C** which depends on the Collector Current and the Base Current. Actually, the Emitter Current is the sum of the Base and the Collector currents:

$$I_E = I_B + I_C$$

But what about the passage width? What is the analogous in a real-life transistor? Well, actually the transistor analogous to this figure is the result of the multiplication of the **h_{FE} hybrid parameter** by the **Base Current I_B**. The h_{FE} parameter is the most important parameter of the transistor. This is the parameter which indicates the current multiplication. We will work quite extensively with this parameter in the following pages. Right now you only need to know and understand the following statement:

A transistor is a **CURRENT DEVICE** used to multiply **CURRENT**. The multiplication factor is called "**Current Gain**" and is represented by the hybrid parameter **h_{FE}**. The output Collector Current is the result of the product of the Base current multiplied by the Current Gain: **$I_C = I_B \times h_{FE}$**

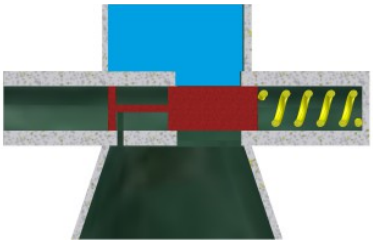

Fig. 1.4 No water flows through the transistor if no control pressure is applied

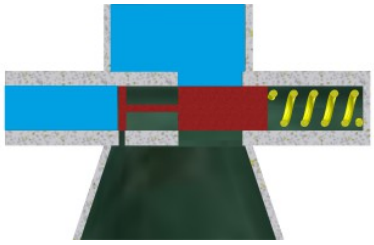

Fig. 1.5 The control pressure must exceed a specific pressure threshold otherwise there is no water flow.

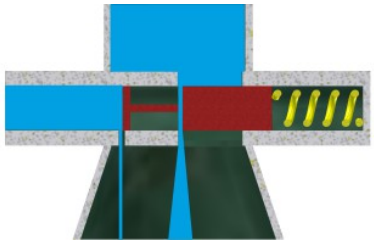

Fig. 1.6 When water flows through the control, the passage between the input and output opens and water flows through

If the pressure in the control is increased, the piston will move even further effectively widening the opening area between the input and the output. This will result in two things: First, the water flow through the control (Base Current I_B) will be increased because the control pressure was increased. Second, the water flow from the input to the output (Collector Current I_C and Emitter Current I_E) will also be increased. This increment is illustrated in figure 1.7. Notice that the flow through the output is many times bigger than the flow through the control. In other words, a small water flow change at the control of the valve results into a large water flow at the output. This sentence best describes the transistor operation:

A small base current change results into a large collector current change

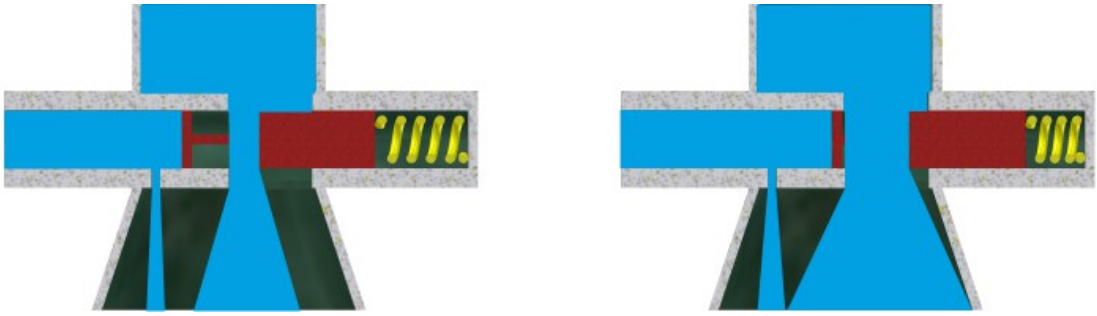

Fig. 1.7 A small flow change through the Control results in a large flow change through the Input-Output

1.2.2 From the Hydraulic Model to the real Transistor

Now let's see how the previous knowledge can be applied into an NPN transistor. Figure 1.8 illustrates how a typical NPN transistor is connected. The Collector-Base contact is reverse-biased with the positive side of the V_{CC} supply connected to the collector (N) and the negative side of the V_{CC} supply connected to the base (P). The Base-Emitter contact is forward-biased with the positive side of the V_{EE} supply connected to the base (P) and the negative side of the V_{EE} supply connected to the emitter (N).

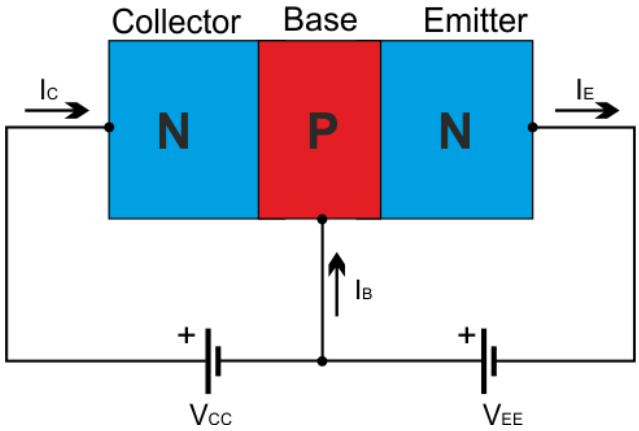

Fig. 1.8 A typical NPN transistor connection

Assuming that the Base-Emitter voltage V_{BE} is larger than the minimum V_{BE} threshold (around 0.6V to 0.7V for a silicon transistor), this connection will cause a small base current I_B to flow from the base to the emitter. An amount of current will flow through the collector to the emitter due to the base current. This collector current I_C is proportional to the base current I_B. The magnitude of the collector current depends on the Current Gain parameter of the transistor (h_{FE}).

Finally, the emitter current is the sum of the base and the collector currents. The two formulas that one needs to remember are these:

$$I_E = I_B + I_C$$

$$I_C = h_{fe} \times I_B$$

1.3 The Hybrid Parameters [h]

The hybrid parameters are values that characterize the operation of a transistor, such as the amplification factor, the resistance and others. They are used to calculate and properly use the transistor in a circuit. Most of the the hybrid parameter values are given in the datasheet by the manufacturer. You do not need to learn everything about hybrid parameters to design a transistor circuit, but it is good to know that they exist. Here is a quick reference:

1.3.1 The Hybrid Parameters for Common Emitter (CE) Connection

Here is the first set of hybrid parameters for a transistor connected with common emitter. For now you do not have to worry about the type of connection. We will discuss them thoroughly in the next chapters.

1.3.1.1 h_{ie} - Input Impedance

The first hybrid parameter that we will see is the h_{ie}. This parameter is defined by the result of the division of the V_{BE} by I_B:

$$h_{ie} = \frac{V_{BE}}{I_B}$$

This parameter defines the input resistance of a transistor, when the output is short-circuited (V_{CE}=0).

1.3.1.2 h_{fe} - Current Gain

This is the most important parameter and is extensively used when calculating a transistor amplifier. This is actually the only parameter you need to know to begin designing amplifiers and other transistor circuits. The equation for this parameter is the following:

$$h_{fe} = \frac{I_C}{I_B}$$

When we have the output of the transistor short-circuited (V_{CE}=0), h_{fe} defines the current gain of the transistor in common emitter (CE) configuration. Using this parameter we can calculate the output current (I_C) from the input current (I_B):

$$I_C = I_B \times h_{fe}$$

This explains why this parameter is so useful. A BJT transistor has typical current amplification from 10 to 800, while a Darlington pair transistor can have an amplification factor of 10.000 or more. Another symbol for the h_{fe} is the Greek letter **β** (spelled "Beta").

1.3.1.3 h_{oe} - Output Conductivity

This parameter is defined with the input open (I_B=0) and the transistor connected in common emitter (CE) configuration. The equation is:

$$h_{oe} = \frac{I_C}{V_{CE}}$$

With the above conditions, this parameter defines the conductivity of the output. So, the impedance of the output can be defined as follows:

$$ro = \frac{1}{h_{oe}} \Rightarrow ro = \frac{V_{CE}}{I_C}$$

1.3.2 The hybrid parameters for Common Base (CB) Connection

1.3.2.1 h_{fb} - Current Gain

As in common emitter configuration, so in common base configuration there is a current gain ratio which is defined by the manufacturer with the h_{fb} parameter. In this type of connection, the current amplification is almost one which means that no practical current amplification occurs. h_{fb} is also symbolized with the Greek letter **α** (pronounced "Alpha").

$$0.9 < \alpha < 1$$

The formula to calculate this parameter is the following:

$$-h_{fb} = \frac{I_C}{I_E}$$

1.3.3 The Hybrid Parameters for Common Collector (CC) Connection

1.3.3.1 h_{fc} - Current Gain

As you understand, the current gain is the most important parameter in every type of connection. The same applies for the common collector connection. The equation is as follows:

$$-h_{fc} = \frac{I_E}{I_B}$$

An alternative symbol for h_{fc} is the Greek letter **γ** (pronounced Gama). For the sake of simplicity the designer can generally use the h_{fe} parameter for his calculations. Remember that I_E is approximately equal to I_C, so we can conclude that h_{fc} is approximately equal to h_{fe}.

1.3.4 Static and Dynamic Operation

As we saw above, the hybrid parameters begin with the letter h, and then a pointer follows to define which parameter we are talking about. If the pointer is written with lowercase letters, then this parameter refers to **dynamic transistor operation**. We call it dynamic operation when the transistor operates with **AC voltage**, for example in an audio amplifier. If the pointer of the h parameter is written with capital letters, then the parameter refers to **static transistor operation**. The transistor operates statically if there is only **DC voltage**, for example in a transistor relay driver.

The current gain parameters have almost the same values in both static and dynamic operation. So we can safely say that h_{FE} is almost equal to $h_{fe.}$ Generally:

$$h_{fe} \approx h_{FE} \quad (\text{although } h_{fe} \neq h_{FE})$$
$$h_{fb} \approx h_{FB} \quad (\text{although } h_{fb} \neq h_{FB})$$
$$h_{fc} \approx h_{FC} \quad (\text{although } h_{fc} \neq h_{FC})$$

For static operation, the alternative Greek letters can be used as well, with the pointer 0 or dc:

$$h_{FE} = \beta_0 = \beta_{dc}$$
$$h_{FB} = \alpha_0 = \alpha_{dc}$$
$$h_{FC} = \gamma_0 = \gamma_{dc}$$

1.3.5 Hybrid parameters are unstable

One of the most common problems that a circuit designer faces when using transistors, is the fact that the h parameters are very sensitive to temperature changes. The most annoying thing about this is that the current gain changes dramatically. In common emitter configuration for example, h_{fe} can increase by 60% if the temperature climbs form 25 to 100 degrees. Also take into account that a transistor dissipates power in the form of heat, so a temperature increment is something common that happens all the time.

Another problem with hybrid parameters is that even between completely identical transistors, they may vary dramatically. You may have two transistors with the same code from the same manufacturer and the same batch (apparently completely identical) and yet one transistor may have h_{fe} 150 and the other 300 (real measurement)! Within the next pages, we will see how a designer can work around with these problems.

CHAPTER 2

Transistor Circuit Essentials
Connection Methods and Base Biasing Techniques

The first step to design a transistor amplifier is to select the most suitable connection method and the most efficient biasing technique. These are the two most important issues that a circuit designer must know in order to start designing an effective transistor circuit.

2 Transistor Circuit Essentials

Before we start talking about the different types of transistor connections, we first need to declare some characteristic sizes and symbols that will be used from now on.

$\mathbf{I_E}$ is the Emitter current, $\mathbf{I_C}$ is the Collector current and $\mathbf{I_B}$ is the Base current. The direction of each current has to do with the type of the transistor (PNP or NPN). The voltage across two leads will be symbolized by the letter **V**, with the two letters of the corresponding leads of the transistor as pointers. The second letter will always be the one that also characterizes the connection type of the transistor. So for example in Common Base connection, the voltage across the emitter and the base is $\mathbf{V_{EB}}$, and the voltage across the collector and the base is $\mathbf{V_{CB}}$. Similarly, in common emitter connection, $\mathbf{V_{BE}}$ is the voltage across the base and the emitter and $\mathbf{V_{CE}}$ is the voltage across the collector and the emitter. We will symbolize the power supplies of the leads with the letter **V** followed by the letter of the corresponding lead, twice. The symbol $\mathbf{V_{EE}}$ is for the emitter supply, $\mathbf{V_{CC}}$ for the collector supply and $\mathbf{V_{BB}}$ for the base supply.

2.1 Choosing the right connection

There are three methods that a transistor can be connected, each one having advantages and disadvantages and specific application uses. So it is very important before you start designing your circuit to be able to select the proper connection according to your application requirements. First we will see these three connections at a glance, and then we will discuss each one thoroughly.

2.1.1 The Common Base (CB) Connection at a Glance

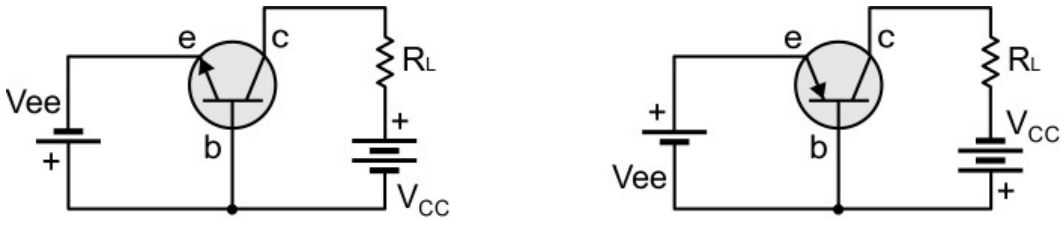

Fig. 2.1 The Common Base transistor connection for an NPN (left) and a PNP (right) transistor

A transistor is connected with common base when the emitter-base diode is forward biased and the collector-base diode is reverse-biased, the input signal is applied to the emitter and the output is taken from the collector. It is called "common base" because the **input and output circuits share the base in common**.

The common base connection is probably the most rarely used type due to some strange behavior that it has. As we saw in the operation of a transistor in the previous chapter, the emitter current is the strongest current of all within a transistor ($\mathbf{I_E = I_B + I_C}$). What this means is that the input of this circuit (emitter) must be able to provide enough current to source the output (collector). Moreover, the output current ($\mathbf{I_C}$) will be slightly less than the input current ($\mathbf{I_E}$). So this connection type is absolutely **improper for a current amplifier**, since the current gain is slightly less than unity ($\mathbf{0.9 < h_{fb} < 1}$), in other words it acts as a **current attenuator** rather than a current amplifier.

On the other hand, it does provide a **small voltage amplification**. The output signal is in phase with the input signal, so we can say that this is a **non-inverting amplifier**. But here comes another strange behavior: The voltage amplification ratio of this circuit is very difficult to be calculated, because it depends on some operational characteristics of the transistor that are difficult to be measured directly. The emitter-base internal resistance of the transistor for example and the amount of DC bias of the input signal play a major role in the final amplification ratio, but these are not the only ones. The current that flows within the emitter changes the internal emitter-base resistance which eventually changes the amplification ratio. This connection type has a unique advantage. Due to the fact that the base of the transistor is connected to the ground of the circuit, it performs a **very effective grounded screen** between the input and the output. Therefore, it is most unlikely that the output signal will be fed back into the input circuit, especially in **high frequency applications**. So, this circuit is widely used in VHF and UHF amplifiers.

2.1.2 The Common Collector Connection (CC) at a Glance (Emitter Follower)

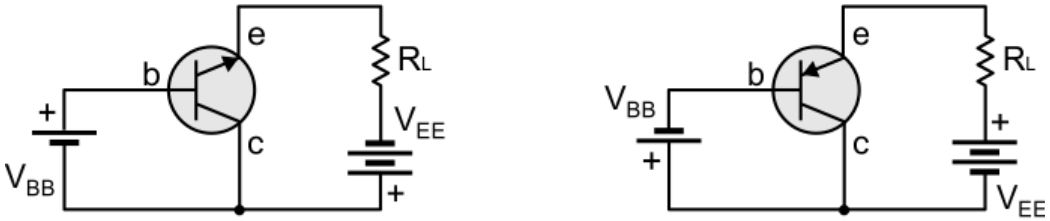

Fig. 2.2 The Common Collector transistor connection for an NPN (left) and a PNP (right) transistor

A transistor is connected with common collector, when the base-collector and emitter-collector diodes are forward biased, the input signal is applied to the base, and the output is taken from the emitter. It is called "common collector" because the input and output circuits share the collector in common.

The common collector connection is used in applications where **large current amplification** is required, without voltage amplification. As a matter of fact, this circuit has the **highest current gain factor**. Remember that $\mathbf{h_{fb} = I_C / I_E}$ (current gain in **CB**), $\mathbf{h_{fe} = I_C / I_B}$ (current gain in **CE**) and $\mathbf{h_{fc} = I_E / I_B}$ (current gain in **CC**). Taking into account that $\mathbf{I_E > I_C}$ ($\mathbf{I_E = I_B + I_C}$) and that $\mathbf{I_B}$ is the smallest current, from the previous three formulas we can easily conclude that $\mathbf{h_{fc} > h_{fe} > h_{fb}}$. The current that this circuit can provide at its output is indeed the highest, and it is the sum of the $\mathbf{I_C}$ current plus the $\mathbf{I_B}$ current from the input.

The most distinctive characteristic though that this connection type has, is that **the output voltage is almost equal to the input voltage**. As a matter of fact, the output voltage will be equal to the input voltage, slightly shifted towards ground ($\mathbf{V_E = V_B - V_{BE}}$). This voltage drop depends on the material that the transistor is made of. A Germanium transistor has $\mathbf{V_{BE} = 0.3V}$ and a Silicon transistor has $\mathbf{V_{BE} = 0.7}$ volts. So, the output signal on a silicon transistor will be exactly the same as the input signal, only that it will be shifted by **0.7 volts**. This is why this connection is also called "**Emitter Follower**". The output signal is in phase with the input signal, thus we say that this is a **non-inverting amplifier** setup.

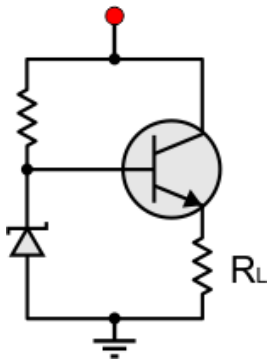

Fig. 2.3 A basic voltage regulator circuit

This is a very efficient circuit to match impedance between two circuits, because this mode has **high input impedance** and **low output impedance**. It is widely used for example to drive the speakers in an audio amplifier, since the speakers have usually very low impedance. It is also used as a current amplifier in applications where the **maximum current** is required, such as driving solenoids, motors etc. This feature makes this type also perfect for designing Darlington pair transistors, since the maximum current amplification is the requirement.

It is also a very effective connection to make **voltage regulators** with high current supply (Fig. 2.3). A Zener diode for example at the base of the transistor will provide a fixed voltage, and the output will be 0.7 volts less than the Zener diode's regulation voltage, since it will follow the input no matter how much current it is called to provide.

2.1.3 The Common Emitter (CE) Connection at a Glance

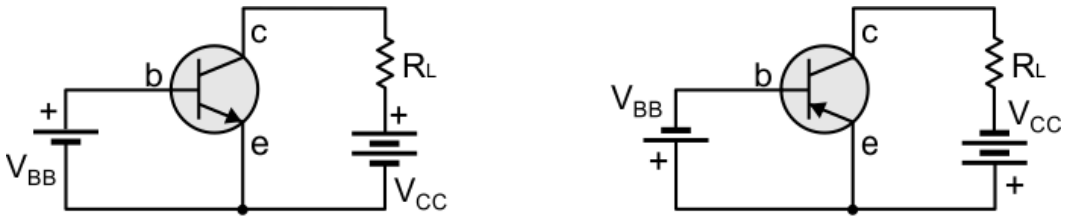

Fig. 2.4 The Common Emitter transistor connection for an NPN (left) and a PNP (right) transistor

A transistor is connected with common emitter connection when the base-emitter and emitter-collector diodes are forward biased. The input signal is applied to the base and the output is taken from the collector. It is called "common emitter" because the input and output circuits share the emitter in common.

This is the most common transistor configuration used. The reason is because it can achieve high current amplification as well as voltage amplification. This results in very high power amplification gain (P = V x I). Although -in maths- the current amplification of a Common Collector circuit is larger than a Common Emitter circuit, typically we can safely say that they both have almost the same gain:

$$h_{fe} = \frac{I_E}{I_B}$$

$$h_{fe} = \frac{I_C}{I_B} \quad (1)$$

$$I_E = I_B + I_C \quad (2)$$

$$(1)(2) \Rightarrow \; h_{fe} = \frac{I_E - I_B}{I_B} = \frac{I_E}{I_B} - \frac{I_B}{I_B} \;\Rightarrow\; h_{fe} = h_{fc} - 1$$

Suppose that a transistor has $\mathbf{h_{fc}=100}$ (in CC). From the above analysis we see that if we connect this transistor with common emitter, it will have $\mathbf{h_{fe}=99}$ ($\mathbf{h_{fc}-1}$), which is not a significant decrement. Additionally, the output voltage can also be predictably amplified. This is what makes this circuit so widely used. We will discuss this specific connection extensively with different biasing techniques.

This mode is used in several applications, such as audio amplifiers, small signal amplification, load switching and more. A distinctive characteristic for this connection is that the output signal has 180 degrees phase difference from the input signal, thus we call it an **inverting amplifier**.

2.1.4 General Connection Characteristics

Here is a table with the characteristic sizes of the three different transistor connections, so that you can directly make your comparisons.

	Common Base	**Common Emitter**	**Common Collector**
Input Impedance	Low (about 50 Ω)	Medium (1-5 KΩ)	High (300-500 KΩ)
Output Impedance	High (500KΩ-1MΩ)	Medium (about 50KΩ)	Low (up to 300 Ω)
Current Gain	Low (<1)	High (50 - 800)	High (50-800)
Voltage Gain	Low (about 20)	High (about 200)	Low (<1)
Power Gain	Low (about 20)	High (up to 10000)	Medium (about 50)

2.2 Choosing the Right Bias

After selecting the proper connection that is most suitable for your application, you must select a biasing method. Biasing in general means **to establish predetermined voltages and currents at specific points of a circuit, so that the circuit components will operate normally**. For transistors, biasing means to **set the proper voltage and current of the transistor base**, thus setting the operating point, also known as **quiescence point (Q)**. We will discuss in details the quiescence point within the next chapters. For now, you need to know that this point will determine how the transistor will operate (amplifier or switch). A correctly placed Q offers maximum amplification without signal distortion or clipping.

The most efficient and commonly used biasing method for transistor amplifiers, it the **Voltage Divider Bias (VDB)**. We will analyze this method in detail, but first we will discuss the other biasing methods. In this chapter, we will use a common emitter NPN transistor amplifier to analyze the various biasing methods but each method can be used for other connections as well.

2.2.1 Fixed Bias

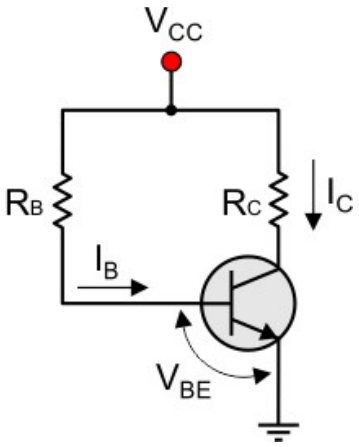

Fig. 2.5 The Fixed Bias is the simplest biasing method, commonly used for switching circuits but rarely in amplifiers

This is the most rarely used biasing method with transistor amplifiers, but it is widely used when the transistor operates as a switch. The base current I_B is controlled by the base resistor R_B. From Kirchhoff's second law we have:

$$V_{CC} = V_{RB} + V_{BE}$$

V_{RB} is calculated using Ohm's law:

$$V_{RB} = I_B \times R_B$$

So, by selecting the proper base resistor R_B, we can define the voltage across the resistor V_{RB} and base current I_B. Now we can calculate the collector current using the appropriate hybrid parameter. Since this is a common emitter circuit, we use the h_{fe}:

$$I_C = I_B \times h_{fe}$$

The problem with this method is that the collector current is very sensitive to slight current gain changes. Suppose for example that this is a silicon transistor and operates as a B-class amplifier with current gain 300, R_B=80 KΩ, R_C=200 Ω and V_{CC} = 10 volts:

$$V_{CC} = V_{RB} + V_{BE} \Rightarrow V_{CC} = I_B \times R_B + V_{BE} \Rightarrow I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{10 - 0{,}7}{80000} = 112.25\,\mu A$$

$$I_C = I_B \times 300 = 33.67\,mA$$

The output of this circuit is taken from the collector resistor RC:

$$V_{RC} = I_C \times R_C = 6.7\,Volts$$

Now suppose that the temperature rises. As we've discussed in earlier pages this will increase the current gain. An increment of 15% is a realistic and rather small. From 300 it will climb up to 345. This means that the collector current will become 38.7mA, and the output voltage will also become 7.7 Volts! A whole volt higher than before. That is why this biasing method is rarely used for transistor amplifiers.

On the other hand, due to the fact that this method is simple and cost-effective, its widely used in **switching applications** (e.g relay driver). That is because the Q point operates from cut-off to hard saturation and even large current gain changes have little or no effect at the output.

2.2.2 Emitter Feedback Bias (Fixed Bias with Emitter Resistor)

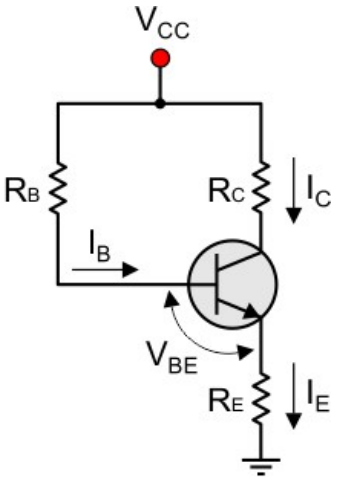

Fig. 2.6 An emitter resistor introduced the first historical negative feedback but still had poor results

This is the first method that was historically used to fix the problem of the unstable current gain discussed previously. In a transistor circuit with fixed bias a resistor was added at the emitter. This method never worked as it should so it is rarely used anymore. This is how it was supposed to work: if the collector current is increased due to a temperature increment, the emitter current is also increased, thus the current through R_E is also increased. The voltage drop across R_E is increased (emitter voltage) which eventually increases the base voltage ($V_B = V_{BE} + V_{RE}$). Finally, this base voltage increment has as a result the decline of the voltage across the base resistor R_B ($V_{RB} = V_{CC} - V_B$), which eventually decreases the current of the base I_B. The idea is that this base current decline also decreases the collector current!

This sounds amazing since a change of the output of the circuit has an effect on the input. This effect is called "**feedback**" and more specifically it is "**negative feedback**", since an output increase causes a decline in input. Here is a formula to calculate the collector current:

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + \frac{R_B}{h_{fe}}}$$

Let's see how the previous circuit would react with a 100 Ohms R_E feedback resistor.

$$I_C = \frac{10 - 0.7}{100 + \frac{80000}{300}} = \frac{9.3}{366.6} = 25.3\,\text{mA}$$

We assume again that the current gain is increased by 15%:

$$I_C = \frac{10 - 0.7}{100 + \frac{80000}{345}} = \frac{9.3}{331.8} = 28\,\text{mA}$$

So, a 15% current gain increase caused a 15.1% output current increase. By adding a 100 Ohms feedback resistor at the emitter, a 15% current gain increase caused a 10.6% output current increment. The increase is 4.5% less which means that this method works somehow, but still the shifting of the Q-point is too large to be acceptable. This is why this method is not so popular.

2.2.3 Collector Feedback Bias (Collector to Base Bias)

The next method that the researchers used to stabilize the Q point is the collector feedback bias. According to this method the base resistor is not connected at the power supply, instead it is connected at the collector of the transistor. If the current gain is increased due to temperature increase, the current through the collector is increased as well, and this decreases the voltage on the collector V_C. But the base resistor is connected at this point, so less current will go through the base resistor. Less current through the base eventually means less current through the collector.

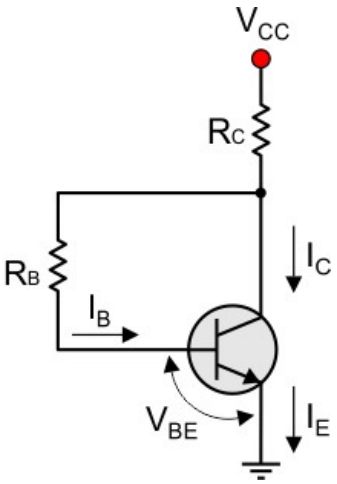

Fig. 2.7 In Collector Feedback Bias the base resistor is directly connected between the collector and its resistor

Again, there is **negative feedback** in this circuit. But how much is it? Lets do some maths. The collector current is now calculated by the following formula:

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + \frac{R_B}{h_{fe}}}$$

To see the change, we will apply this formula in our first example (fixed bias):

$$I_C = \frac{10 - 0.7}{100 + \frac{80000}{300}} = \frac{9.3}{366.6} = 25.3\,\text{mA}$$

When the current gain is increased by 15%:

$$I_C = \frac{10 - 0.7}{100 + \frac{80000}{345}} = \frac{9.3}{331.8} = 28\,\text{mA}$$

The effectiveness of this method compared to the emitter resistor feedback bias shown before is exactly the same. The difference is that RC is usually much larger than RE which results in higher stability. Nevertheless, quiescence point Q cannot be considered stable.

2.2.4 Collector Emitter Feedback Bias

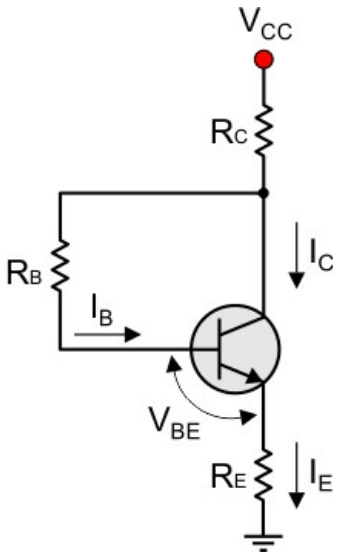

Fig. 2.8 The Collector Emitter Feedback Bias is a hybrid with two negative feedback sources sacrificing amplification gain for the sake of better stability.

It did not take long before someone tried to mix both the previous methods to work together to achieve better results. And indeed, the stabilization is much better than each one separately. The formula to calculate the collector current is the following:

$$I_C = \frac{V_{CC} - V_{BE}}{R_C + R_E + \frac{R_B}{h_{fe}}}$$

Let's apply this formula to our previous examples:

$$I_C = \frac{10 - 0.7}{100 + 100 + \frac{80000}{300}} = \frac{9.3}{466} = 19.9\,\text{mA}$$

With a 15% current gain increase:

$$I_C = \frac{10 - 0.7}{100 + 100 + \frac{80000}{345}} = \frac{9.2}{431.8} = 21.3\,\text{mA}$$

So, a 15% current gain increment causes a 7% output current increase. Although it is better than the previous circuits, still the Q point is not stable enough. Add to this that h_{fe} is extremely sensitive to temperature changes and the transistor generates a lot of heat when it operates as a power amplifier. So we need a much better stabilization technique.

2.2.5 Voltage Divider Biasing

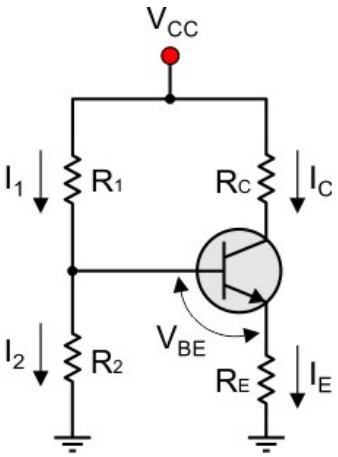

Fig. 2.9 The Voltage Divider Biasing technique is the most effective biasing method for transistor amplifiers

The most effective method to bias the base of a transistor amplifier is using a Voltage Divider. In the next chapter we will analyze each transistor connection in detail and we will be always using this biasing method. Therefore let's take some time to explain this method thoroughly.

The idea is that the voltage divider maintains a very stable voltage at the base of the transistor and if the base current is many times smaller than the current through the divider, the base voltage remains practically unchanged. The resistor R_E provides the negative feedback as explained before (Emitter Feedback Bias). Due to the fact that the base voltage remains unchanged, the negative feedback works very effectively and any unwanted increase in the current gain produces an almost equal negative feedback. The collector and emitter currents change just a little, and the Q point remains practically stable. Now, let's see in detail how this works...

2.2.5.1 Voltage Divider Bias Equations

We start with the assumption that the base current (I_B) is many times smaller than the current through the voltage divider (I_{VD}). Later on we will discuss how to achieve this. A ratio of 20 is a good approach. This means that the base current must be at least 20 times smaller than the voltage divider current. This condition allows us to exclude I_B from our calculations with an error of less than 5%. Now we can safely calculate the base voltage as follows:

$$V_B = I_{VD} \times R_2$$

Or using the classic voltage divider equation:

$$V_B = V_{CC} \frac{R_2}{R_1 + R_2}$$

The current that flows through the voltage divider is (with I_B excluded):

$$I_{VD} = \frac{V_{CC}}{R_1 + R_2}$$

From the base voltage we can calculate the emitter voltage and the collector-emitter voltage drop as follows:

$$V_E = V_B - V_{BE}$$
$$V_{CE} = V_C - V_E$$

The emitter current is calculated using Ohm's law:

$$I_E = \frac{V_E}{R_E}$$

And since the collector current is practically equal to the emitter current we can calculate all the transistor currents and voltages:

$$V_{RC} = I_C \times R_C$$
$$V_C = V_{CC} - V_{RC} = V_{CC} - I_C \times R_C$$
$$V_{CE} = V_{CC} - I_C \times R_C - I_E \times R_E = V_{CC} - I_C \times (R_C + R_E)$$

As you see, we can calculate everything we need **without using any hybrid parameters**. This is an amazing and rather unexpected result. Two transistors with different current gains can operate as amplifiers with exactly the same biasing currents, only because they are biased with a Voltage Divider.

Moreover since V_{BE} is many times smaller than $V_{B,}$ and V_B remains unchanged all the time, the emitter voltage V_E remains unchanged hence maintaining a very stable emitter current.

2.2.5.2 Firm and Stiff Voltage Divider

Previously, we made the assumption that the voltage divider current I_{VD} is many times bigger than the base current I_B, about 20 times as big. This is a good approach for an error less than 5%. This is not always possible though. If the base current is high, the resistor values for the voltage divider must become very small, and this leads to numerous problems.

In such cases we design the voltage divider with a ratio of 10 instead of 20. This approach has an error of less than 10% when the I_B is excluded from the calculations, which is still acceptable. The voltage divider that satisfies this condition is named **Firm Voltage** divider:

$$I_{VD} > 10 \times I_B \Rightarrow R_{VD} < 0.1 \times \beta_{dc} \times R_E$$

On the other hand, the application may require a very good Q stability with an error less than 1%. A ratio of 100 can be used to calculate the resistors if this is possible:

$$I_{VD} > 100 \times I_B \Rightarrow R_{VD} < 0.01 \times \beta_{dc} \times R_E$$

The voltage divider that satisfies this condition is named **Stiff Voltage Divider** and has an error of less than 1%.

2.2.5.3 Condition Confirmation

Suppose that the designer wants to design a transistor amplifier with stiff Voltage Divider Bias. He designs a circuit that has emitter current I_E=1 mA. The voltage divider is calculated according to the stiff VDB condition which means that the base current must be 100 times smaller than the Voltage Divider current. According to this calculation the maximum base current cannot be greater than 40μA. The question now is: does this circuit works efficiently for the whole h_{fe} range?

The fact that I_B and h_{fe} are excluded from the calculations does not mean that these values do not affect the operation. They still have a small affect but this is very small indeed(1 to 10%). What we have to confirm now is that this affect will always remain small, even in the worst case scenario.

But what is the "worst case scenario"? Well, simply: The worst case scenario is when the transistor operates with minimum current amplification. When this happens, the base current becomes maximum to supply the required emitter current. Suppose that the transistor that our designer used has an h_{fe} with a range from 30 to 300. We have to confirm that the base current will remain under the calculated value (40μA) and it still will be able to provide full emitter current (1mA), even at the lowest h_{fe} (30):

$$I_E = \beta \times I_B \Rightarrow I_B = \frac{I_E}{\beta} = \frac{1\,mA}{30} \Rightarrow I_B = 33\,\mu A$$

So, the base current for the worst case scenario (33μA) is still less than the calculated base current (40μA), therefore we can say that this voltage divider remains stiff. This process is called "**Condition Confirmation**" and is used to determine if the circuit satisfies the stiff or firm voltage divider bias condition.

2.2.5.4 What Each Part Does

Designing a transistor amplifier with VDB (Voltage Divider Bias) is not very hard but sometimes it takes time to select the proper part values to begin with. Many times the designer has to change some parts to change the amplifier parameters. Here is a quick reference for the designer to know what each part controls:

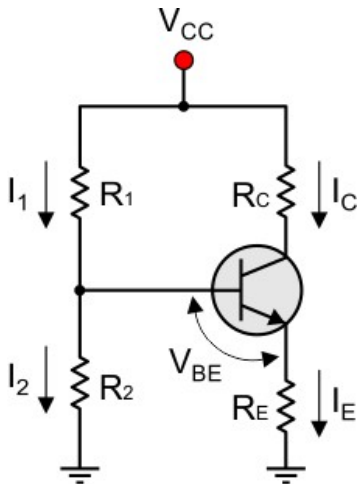

Fig. 2.10 Its good to know which part to change in order to alter a specific bias characteristic of the amplifier

- **R**1 - This resistor controls the current through the voltage divider
- **R**2 - This resistor controls the base voltage V_B
- $\mathbf{R_E}$ - This resistor controls the emitter current I_E
- $\mathbf{R_C}$ - The collector resistor can control the V_{CE} voltage

CHAPTER 3

Output Characteristic, Load Line and Quiescence Point

We are are now entering the circuit analysis of a transistor amplifier. In this chapter we will discuss the method to analyze a transistor DC biasing circuit. This is the second step to design an effective transistor amplifier. We will learn how to choose the right biasing resistors to set the quiescence point Q at the right point to have the amplifier operating with the desired characteristics.

3 Output characteristic, Load Lines and Quiescence Point

There is a very interesting methodology to graphically analyze the operation of a transistor amplifier using the output characteristics and the load lines. By properly setting the quiescence point along the load line one can determine how the transistor amplifier will operate. For example, the same transistor can implement a Hi-Fi audio amplifier, a B-class amplifier or a load switch simply by setting the quiescence point into different positions.

3.1 The DC Load Line.

If you open a transistor datasheet you will probably find a set of diagrams and characteristics. One of these is the **Common Emitter Output** characteristic or **I_C to V_{CE} Characteristic** and looks like this:

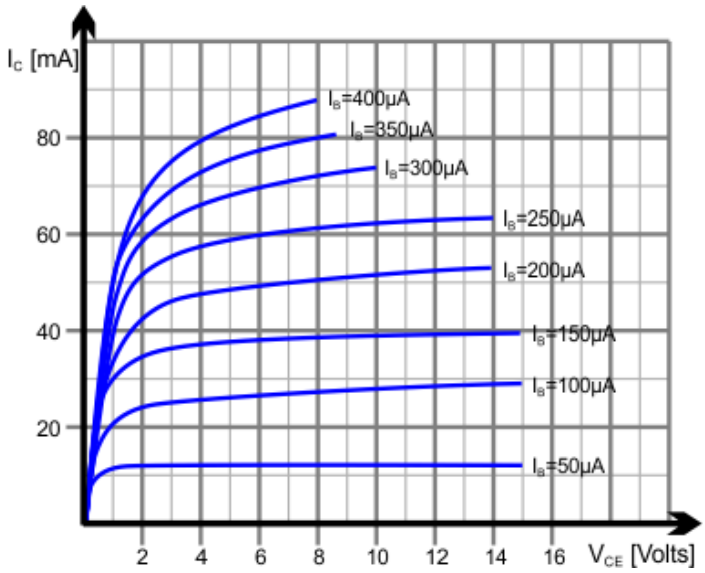

Fig. 3.1 A typical Common Emitter output characteristic

This is the I_C to V_{CE} characteristic of a BC547 transistor. The horizontal axis (x) has the V_{CE} voltage in volts and the vertical axis has the I_C current, usually in milliamperes. Between them, there are several different curves. Each one of these characteristics corresponds to a different base current usually measured in microamperes. From now on we will work extensively with these characteristics, so it is important for you to understand how to read them and how to use them to determine the operation of the amplifier.

The DC Load Line is a line that we draw on these characteristics, which eventually determines all the points that the transistor will operate at. In other words, the operation point (usually called Q from the word "Quiescence") will be somewhere on the DC load line. We use the term "DC" because as we will see in the next chapter, there is also an AC load line. Many times

when we talk about the DC load line, we omit the term "DC" and we write only "Load Line" meaning the "DC Load Line". To draw this load line, we need to know the collector current and the collector-emitter voltage. Suppose for example that I_C=40mA and V_{CE}=12V. The load line is drawn with red color:

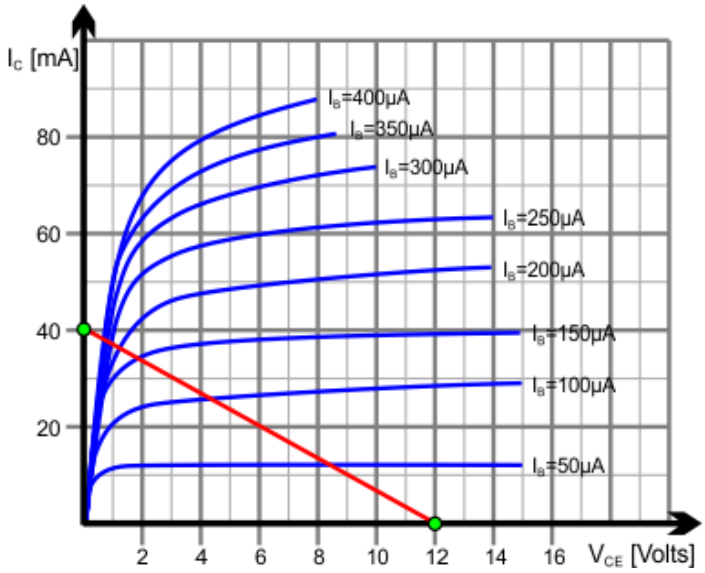

Fig. 3.2 Drawing a Load Line on the Common Emitter output characteristic

We will explain how to draw the load line, but before we do, we must first discuss about the four basic regions of this characteristic, the **saturation area**, the **cut-off area**, the **linear area** and the **breakdown point**.

3.1.1 Region 1: The Saturation Area

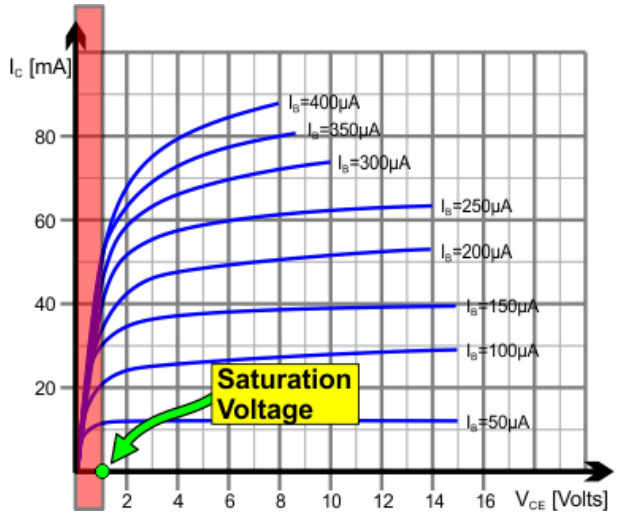

Fig. 3.3 When the transistor operates in the Saturation Area the collector current is maximized

The Saturation Area is the area in which the collector current increases rapidly. Figure 3.3 illustrates this area (with red mask). Typically we consider that the saturation area starts from 0.5 V_{CE} and bellow. This voltage is called "**Saturation Voltage**". Drawing the load line reveals that the saturation area covers the highest current regions of the load line. This explains why a saturated transistor (as we generally call it) provides maximum output current.

If the collector current is very high, the collector contact of the transistor is overheated and eventually the transistor is destroyed. Therefore, if the transistor is planned to operate at the saturation area (usually for switching applications), caution must be taken to maintain the collector current bellow harmful levels.

If the transistor operates as an amplifier and it is driven in the saturation area, then the output signal is distorted. That is because the transistor operates in an area that the V_{CE} to I_C change is not linear. To avoid this the transistor amplifier must be calculated in a way that the collector-emitter voltage will not fall bellow the saturation voltage. Generally:

$$V_{CE} > 0.5\,\text{Volts}$$

3.1.2 Region 2: The Cut-Off area

The cut-off area is the area in which the collector current becomes zero. In the following drawing, the cut-off area is marked with yellow mask:

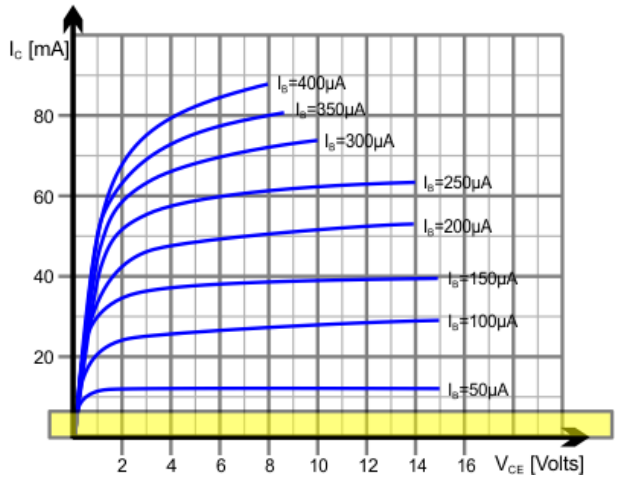

Fig. 3.4 When the transistor operates in the Cut-Off Area the collector current is practically zero

Generally, we can say that in order for a transistor to work in the cut-off area, the base current I_B must become zero. This comes out of the I_C to I_B equation:

$$I_C = \beta \times I_B$$

The precise equation to calculate the cut-off point is this:

$$I_B = \frac{I_{C0}}{1-\alpha} + \beta \times I_B$$

I_{CO} is the reverse saturation current. Since it is very small, usually around 10 to 50nA, we can safely remove it from the previous equation.

When a transistor operates in the cut-off area, no current flows within the collector. Usually we drive the transistor in this area when we want it to operate as a switch. If the transistor operates as an amplifier, then the output signal will be clipped.

3.1.3 Region 3: The Linear Area

The linear area is the area between the cutoff and saturation area of the transistor as shown in Figure 3.5 with a green mask.

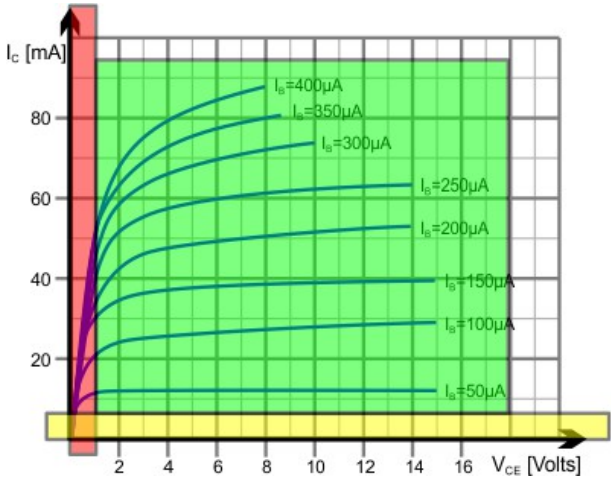

Fig. 3.5 The Linear Area (green) is where the transistor operates as a linear amplifier

It is called "linear area" because in this area the transistor has the most linear operation. To successfully design a transistor amplifier the designer must be able to set the transistor to work within this area, otherwise the output signal will be either clipped or distorted. There are though occasions where an amplifier operates beyond the linear area, such as a class-B or class-C amplifier.

On the other hand, if the transistor operates as a switch, it must not operate within this area. A switch must be either ON or OFF, and this can only be achieved if the transistor operates in the saturation or cutoff areas.

3.1.4 Region 4: The Breakdown Point

The breakdown point is the point on the V_{CE} axis above which the collector current increases rapidly and the transistor is destroyed. This area is marked with a purple mask in figure 3.6:

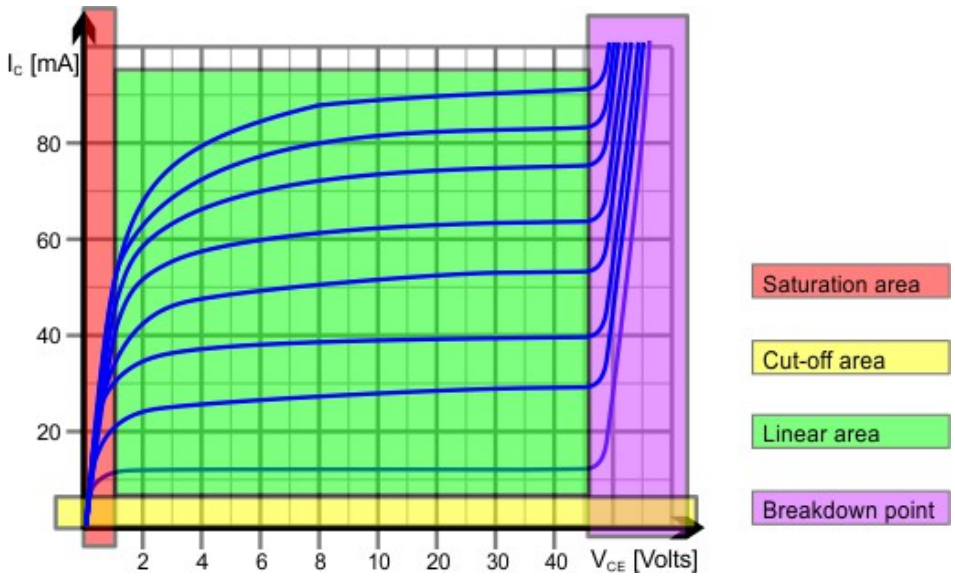

Fig. 3.6 If the transistor is driven above the Breakdown Point (purple area) the collector current increases rapidly and the transistor is destroyed

3.2 How to draw the Load Line (DC Load line)

To get a first clue about the Load Line, We will use an example with a Common Emitter amplifier with Voltage Divider Biasing. More details are yet to come. Here is the circuit:

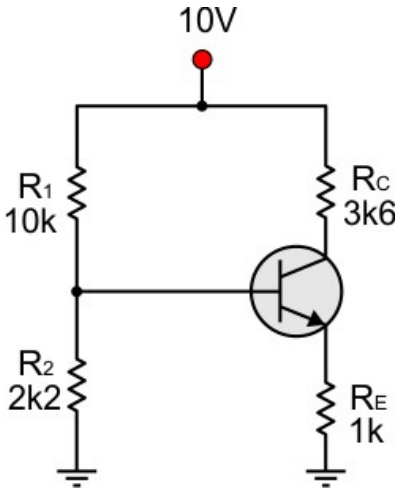

Fig. 3.7 We will use this circuit to draw the Load Line

For an instance, let's just forget about the input portion of the circuit (the Voltage Divider) and let's work only with the output portion. According to Kirchhoff s' law we have:

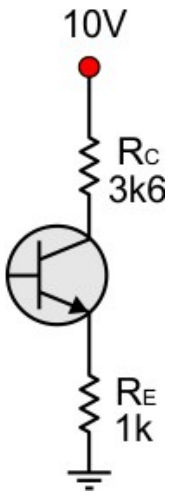

Fig. 3.8 The output portion of the circuit of figure 3.7

$$V_{CC} = I_C \times R_C + V_{CE} + V_E$$

Let's now calculate the first point of the load line. This point (like any other point in ax X-Y Cartesian system) has 2 terms: an X and a Y term. We need to find a V_{CE} and a I_C pair of values which corresponds to the X and Y terms respectively. We can make this calculation much easier with a simple and common trick: We will calculate a V_{CE} value for I_C=0. This way, the first pair will be on the V_{CE} axis. Let's solve the previous equation for V_{CE}:

$$V_{CE} = V_{CC} - I_C \times R_C - I_E \times R_E$$

First thing that we notice is that I_C x R_C is zero, since I_C is zero. V_E is zero as well, because I_E is equal to I_C (approcimately). The equation can be re-written as follows:

$$V_{CE} = V_{CC} - 0 - 0 \;\Rightarrow\; V_{CE} = V_{CC} = 10\,\text{Volts}$$

Now for the second pair. Similarly, we will calculate a I_C value for $V_{CE} = 0$. So, the second point will be on the I_C axis. Let's solve for I_C:

$$V_{CC} = I_C \times R_C + V_{CE} + I_E \times R_E = I_C \times R_C + V_{CE} + I_C \times R_E = I_C \times (R_C + R_E) + V_{CE}$$

$$\Rightarrow I_C = \frac{V_{CC} - V_{CE}}{R_C + R_E}$$

And since we defined that $V_{CE} = 0$:

$$I_C = \frac{V_{CC}}{R_C + R_E} = \frac{10}{4600} = 2.17\,\text{mA}$$

So, now we have the 2 points required. The points are:

- **Point A (10, 0)**
- **Point B (0, 2.17)**

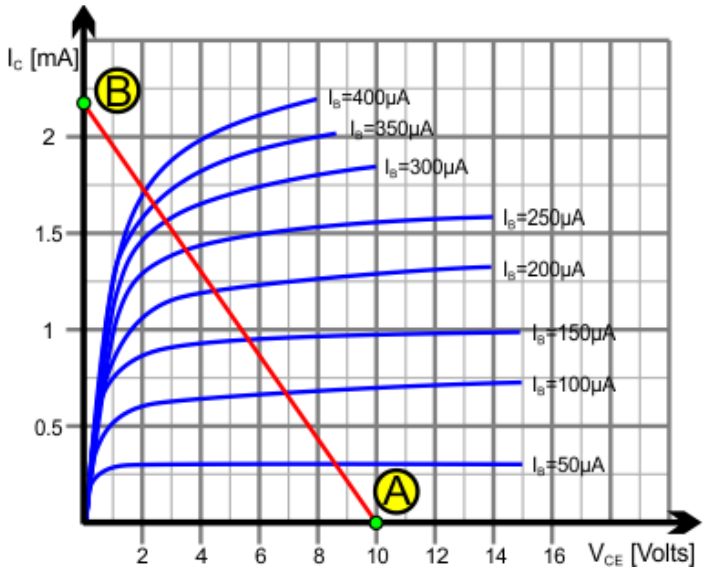

Fig. 3.9 The circuit of figure 3.7 has this Load Line

The green dots indicate the 2 points of the load line, and the red line is the DC load line itself. The quiescence point will be located somewhere on this load line.

3.3 The Operation Point, AKA Quiescence Point - Q

We will continue the previous example and we will calculate the quiescence point - Q. There is something that we need to make clear: The Q point is **a point on the Load Line**. The Load Line is calculated (as we saw before) by finding two points in the cut-off and saturation area. **The Q point is determined by the DC biasing of the transistor**. The fact that the circuit uses VDB (Voltage Divider Bias), allows us to neglect the base current in our calculations. So, the base voltage is:

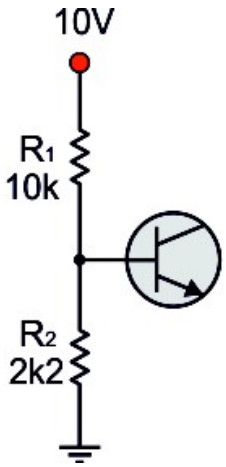

Fig. 3.10 The input portion of the circuit of figure 3.7

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2} = \frac{10 \times 2200}{12200} = 1.8\,\text{Volts}$$

We can now calculate the emitter voltage as follows:

$$V_E = V_B - V_{BE} = 1.8 - 0.7 = 1.1\,\text{Volts}$$

And the emitter current is:

$$I_E = \frac{V_E}{R_E} = \frac{1.1}{1000} = 1.1\,\text{mA}$$

And since the collector current is equal to the emitter current, we can calculate the voltage drop across R_C as follows:

$$V_{RC} = I_C \times R_C = I_E \times R_C = 1.1 \times 6300 = 3.96\,\text{Volts}$$

Finally, the collector emitter voltage is calculated as follows:

$$V_{CE} = V_{CC} - V_{RC} - V_E = 10 - 3.96 - 1.1 = 4.94\,\text{Volts}$$

Now we have everything we need to set the Q point:

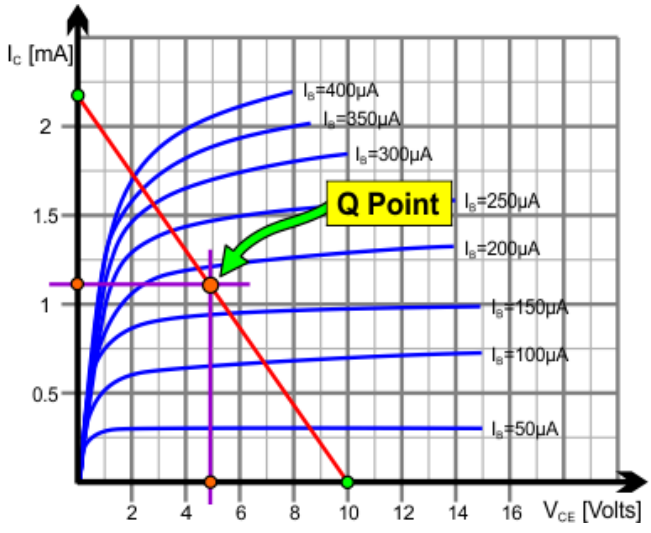

Fig. 3.11 The Q point is always located somewhere on the load line

- **I_C = 1.1 mA**
- **V_{CE} = 4.94 V**

Let's analyze for a moment what we've done so far. First, we calculated the two points to draw the load line. The first point was located on the V_{CE} axis by zeroing the I_C current, and the other point was located on the I_C axis by zeroing the V_{CE} voltage. Both points were calculated with the same equation:

$$V_{CC} = I_C \times R_C + V_{CE} + V_E$$

For the first point we solved this equation for V_{CE}, and for the second we solved it for I_C. Then, we calculated the Q point. For the Q point, we need another pair of I_C - V_{CE} values. These values are calculated **from the DC transistor bias**. If the DC bias is not in the cut-off or in the saturation area, then it must be somewhere on the DC load line that we draw before. That is true since both the load line points and the quiescence point are calculated with the exact same equation. The only difference is that for the load line, we choose (for our own convenience and only) to find points on the two axis, whilst for the quiescence point we solve the equation for the DC values defined by the biasing resistors.

Since the quiescence point is only one, and since the I_C and V_{CE} values of the quiescence point are critical, we usually use the pointer "q". So, for the quiescence V_{CE} voltage we use the symbol V_{CEq}, and for the quiescence I_C current we use the symbol I_{Cq}.

CHAPTER 4

The Transistor Operation in AC
The Coupling and Bypassing Capacitors

So far we've learned how to connect and bias the transistor, as well as we've learned how to properly set the load line and the quiescence point. Up until now, we've been only working with DC supplies. Its now time to feed the AC signal into our amplifier!

In this chapter we will discuss about the AC passive components - namely the coupling and bypassing capacitors. We will size the proper components to ensure efficient and stable operation.

4 The Transistor operation in AC

Until now, we've been talking only for transistors in DC operation. We've learned how to bias a transistor correctly, and we also saw a quick example on how to set the operation point. But many times, transistors are meant to operate with AC signals. A transistor audio amplifier for example is an AC signal amplifier, since the microphone generally generates an AC output. And here is a point that many people confuse: **Transistors are NOT AC components**: Transistors can only operate with DC signals!

That sounds kinda weird, since we all know that transistors are also used to amplify AC signals. But think about this: Suppose that we have an NPN common emitter transistor amplifier, and we feed an AC signal at its base. As long as the input signal is higher than 0.7 Volts, it will be amplified normally and it will appear at the output of the amplifier. But what happens when the signal becomes less than 0.7 Volts? And worst, what happens when the signal becomes negative? As we know, an AC signal has a positive and a negative period.

A negative signal at the base of an NPN transistor means that the base-emitter diode is reverse-biased. The diode acts like an open circuit (cut-off) and the amplifier does not work at all. There is also a tight limit: If the negative voltage become too high, the base-emitter diode will be destroyed. The maximum reverse voltage that this diode can handle is usually around 5 volts for common transistors. The exact value for each transistor can be found in the manufacturer's datasheet, usually with parameter name V_{EBO} (emitter base voltage). The same situation happens of course if we use a PNP transistor and we reverse-bias the base-emitter diode.

So, how is it possible to amplify an AC signal? The answer is by biasing the transistor with DC voltage. Suppose for example that we want to amplify a 1 Vp-p AC signal. This means that the signal has +0.5 Volts positive period and 0.5 Volts negative period. If we bias the input with let's say 1.5 Volts DC, then the input will vary from 2 Volts (1.5 + 0.5) to 1 Volt (1.5 - 0,5). This is considered as a DC signal and the transistor can amplify the complete period normally.

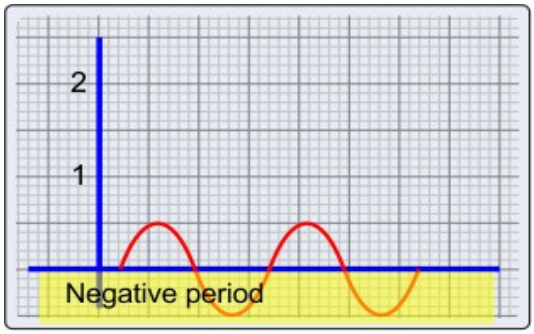

Fig. 4.1 A typical 1 Vp-p AC signal oscillates from +0,5V to -0.5V

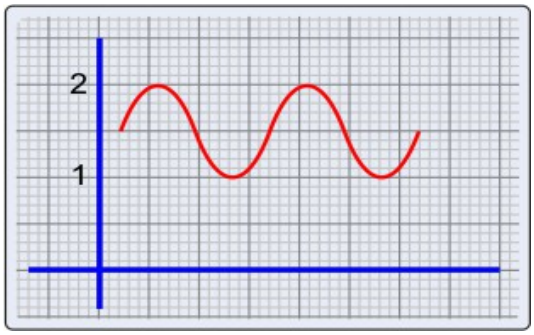

Fig. 4.2 Shifting up the signal with a 1.5V DC turns it into a DC with no negative portion

In figure 4.1 an 1Vp-p AC signal is illustrated. Feeding this signal into the base the transistor will not be amplified correctly since it has a negative period as well. In figure 4.2, the base of the transistor is biased with 1.5 Volts DC supply. The AC signal is therefor shifted upwards eliminating any negative period. The signal of figure 4.2 will be amplified normally.

4.1 Coupling and Bypassing Capacitors

As we said before, transistors are DC components. This means that the output will also be a DC voltage. But if we amplify an AC voltage, then we probably want to get an AC voltage at the output as well. How is this done? Simple, with a coupling capacitor. A capacitor operates as a resistor in AC and as a strict open circuit in DC. It is not the purpose of this theory to analyze in details the capacitor's behavior in AC and DC. Nevertheless, it is important to have some basic knowledge about capacitors.

4.1.1 The Coupling Capacitor

A coupling capacitor is a capacitor connected in series with the circuit that we want to couple. The AC signal is free to go through the capacitor, while the same capacitor acts as an open circuit **effectively blocking any DC current**. Let's see an example of a coupling capacitor:

Both C_{IN} and C_{OUT} in figure 4.3 are coupling capacitors. Their job is to block any unwanted DC currents from between the stages that they couple. Figure 4.4 is what would appear in the oscilloscope's screen if two channels were connected, one before the C_{OUT} coupling capacitor (Channel 1-Blue line) and one after the same capacitor (Channel 2-Red line).

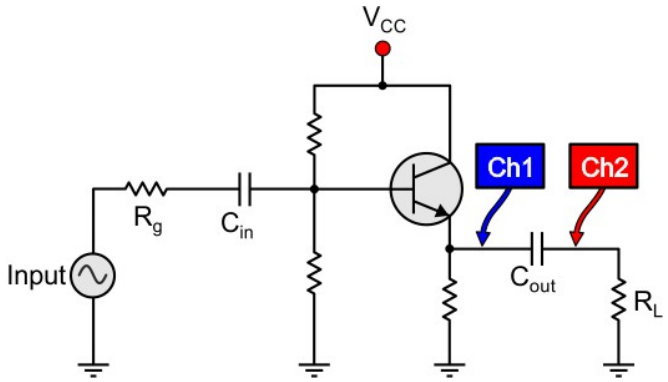

Fig. 4.3 C_{IN} and C_{OUT} are coupling capacitors blocking unwanted DC currents

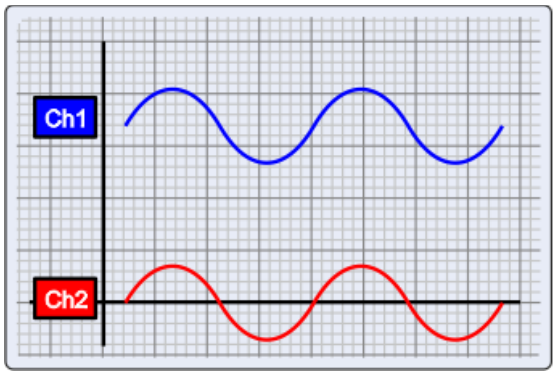

Fig. 4.4 The coupling capacitor removes any DC.

Looking at Channel 1, it is obvious that the amplified AC voltage has been shifted above the zero line, and has become a DC voltage. That is because the DC voltage from the emitter of the transistor has been added to the amplified AC signal. Looking at channel 2, any DC voltage has been removed due to the coupling capacitor. It is possible only for the AC voltage to cross, and therefore it has become an AC voltage again.

4.1.2 The Bypassing Capacitor

A bypassing capacitor is a capacitor connected in parallel with a circuit that we want to bypass. Unlike the coupling capacitor, the bypassing capacitor **removes any unwanted AC signal** from this circuit, since any AC current goes through the bypassing capacitor, leaving only the DC current to go through the parallel circuit. Let's see an example:

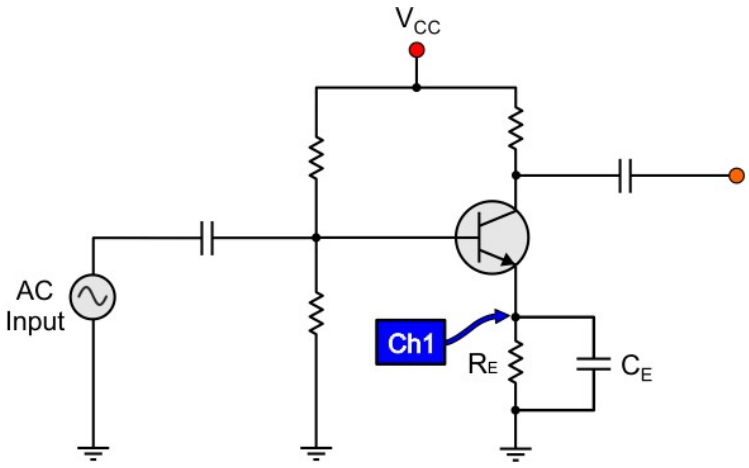

Fig. 4.5 Bypass capacitor C_E is used to bypass any AC current so that the parallel load R_E is not affected

A bypass capacitor (C_E) is connected in parallel with a resistor (R_E). What we want is to have only DC current flowing through the resistor, in order to maintain the voltage stable ($V_E=I_E*R_E$). The problem is that when an AC signal is applied at the base of this circuit, this AC signal will also **appear at the emitter** of the transistor. This will change the emitter current which will eventually change the emitter voltage, and we do not want that. Therefore, we add the bypassing capacitor C_E. The majority of the AC voltage will be grounded through this capacitor. Hence, the current across the resistor R_E will not change, and the voltage will remain stable. In the following graphs (4.6 & 4.7) you can see what would appear in an oscilloscope's screen, if the probe was connected across R_E. The left graph shows the output without a bypassing capacitor, and the right graph shows the output with the bypassing capacitor C_E connected across R_E:

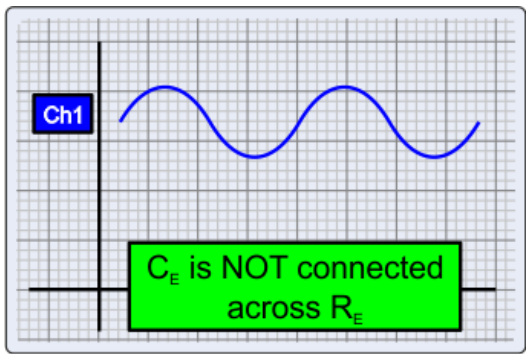

Fig. 4.6 Probing across the feedback resistor R_E (Ch1) . The input AC signal appears across the feedback resistor causing the Q point to oscillate.

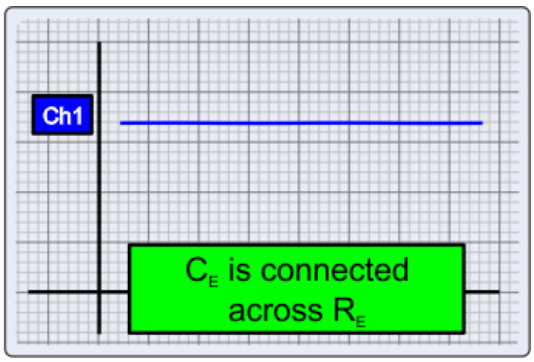

Fig. 4.7 The bypassing capacitor C_E is connected across the feedback resistor R_E. AC current flows through the capacitor because it has less resistance than R_E in AC. The voltage across R_E is now virtually stable

4.1.3 Sizing the Capacitors

In order for a coupling or bypassing capacitor to operate effectively, it must have the right size. As said before, the capacitor acts like a resistor in AC current. The resistance of a capacitor is called "**impedance**". Unlike resistors, capacitors do not have a fixed impedance. Instead, the impedance is determined by the frequency of the AC signal. The equation to calculate the impedance is the following:

$$X_C = \frac{1}{2 \times \pi \times f \times C}$$

C is the capacitance in Farads, and f is the AC signal frequency in Hertz. So, a 10μF capacitor connected in series with a 1 KHz signal, will present an impedance of:

$$X_C = \frac{1}{2 \times 3.14 \times 1 \times 103 \times 10^{-6}} = 15.9\ \Omega$$

So, what is the proper value for a coupling or a bypassing capacitor? There are two factors that must be taken into account: The frequency and the circuits total resistance. Let's talk about the frequency first. If the amplifier operates as a signal amplifier of a fixed frequency, then the answer is straight-forward: The frequency is the signal's frequency. But if the amplifier operates in a wide frequency range, then we must choose the worst case scenario.

Let's see an example of an audio amplifier. Audio amplifiers typically operate from 20Hz up to 20Kz. To choose the right frequency for our calculation, we must first think what we want the bypassing or coupling capacitor to do: We want this capacitor to act as a short-circuit in AC currents. In other words, we want the capacitor to present the **lowest impedance possible** in AC current. Since the impedance X_C is reverse-proportional to the frequency F, the lowest impedance is presented **at the highest frequency**. Thus, the worst case scenario (highest impedance) is presented at the **lowest frequency**. So, in our calculations we will **use the lowest frequency** that the capacitor will operate at. In an audio amplifier for example the lowest frequency is 20Hz.

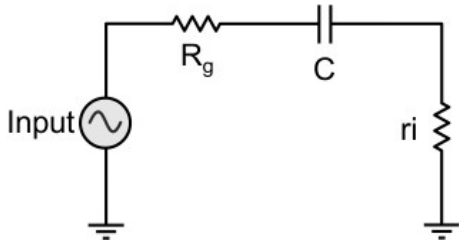

Fig. 4.8 The total circuit resistance that a coupling capacitor C is connected to is the sum of all series resistances (Rg+ri)

The second factor is the total resistance of the circuit. Let's talk first for a coupling capacitor. In this case, we are talking about the total resistance of the circuit in series with the capacitor. Check out the schematic of figure 4.8. In this circuit, the total resistance is the sum of the internal resistance of the generator Rg, plus the internal resistance of the transistor ri.

If the capacitor operates as a bypassing

capacitor (like the schematic of figure 4.9), the total resistance is refereed to the total resistance of the circuit parallel to the bypassing capacitor – in our example this is the emitter resistor R_E.

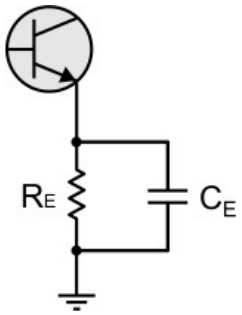

Fig. 4.9 The total resistance that a bypassing capacitor is connected to is the series of all parallel loads to the capacitor.

So, now we know how to choose the worst case scenario in terms of frequency, and how to calculate the total circuit resistance according to the capacitor type (coupling or bypassing). The optimum capacitor value that we choose should be at least **10 times smaller than the total circuit resistance**, calculated for the worst case scenario. To calculate the capacitor, we solve the impedance equation for C:

$$C = \frac{1}{2 \times \pi \times f \times X_C}$$

Let's see an example. In figure 4.8, Rg is 50 Ohms. ri is 2,2 KΩ and the frequency range is 20Hz to 20KHz. To calculate the optimum capacitor value, we must first calculate the total resistance of the circuit in series with the capacitor:

$$R_{total} = 50 + 2200 = 2250\,\Omega$$

The worst case scenario is 20Hz (lowest frequency), so the capacitor must present a resistance of less than 225.0 Ω (R_{total} / 10) at 20Hz frequency:

$$C = \frac{1}{2 \times 3.14 \times 20 \times 225} = 35.3\,\mu F$$

So, the capacitor must have at least 35.3uF capacitance. This makes sure that the capacitor will have less than 1% effect on the total resistance of the circuit. And since the calculated value does not exist as a standard capacitor value, we choose the next bigger value - in our case that is 47 μF.

4.2 The DC and AC Equivalents

As we said previously, a transistor amplifier usually operates both with AC and DC voltages, the DC voltage is used to bias the transistor and the AC voltage is the signal that will be amplified. To analyze a transistor circuit, both voltages must be analyzed. But the transistor itself as well as the biasing components react different in AC and DC signals. Obviously, there must be a method to analyze each signal separately. The simplest and most widely used method is using the DC and AC equivalents. According to this method, two equivalent circuits are extracted from the original circuit, the DC and the AC equivalent. The currents and voltages for each circuit are calculated separately, and then, using the superposition theorem we can calculate the final values. For your information, the superposition theorem states that:

"The response -voltage or current- in any branch of a bilateral linear circuit having more than one independent source, equals the algebraic sum of the responses caused by each independent source acting alone, while all other independent sources are replaced by their internal impedances."

4.2.1 The DC Equivalent

To make the DC equivalent circuit, the following steps must be taken:

- I] **All AC sources become zero**
- II] **All capacitor are replaced with an open circuit**

Suppose for example that we have the following circuit in figure 4.10 from which we want to make the DC equivalent:

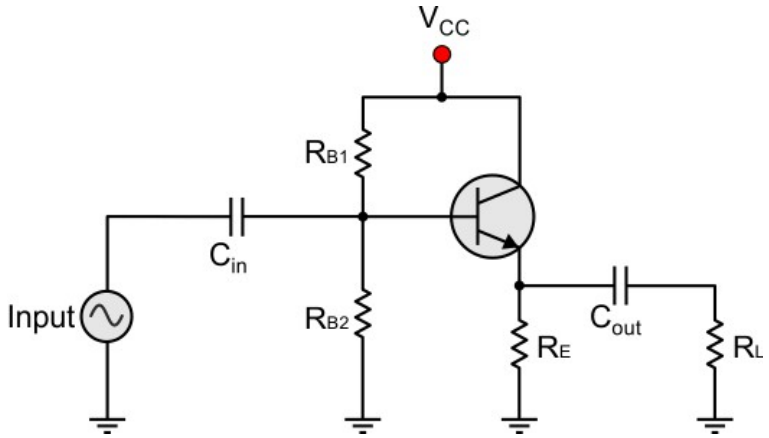

Fig. 4.10 We want to make the DC equivalent circuit out of this one

According to the first rule, all AC sources (if any) must become zero. This applies for the "Input" AC source that we have. When a power source becomes zero, it means that the output voltage will always have the same potential as the grounding signal - which is zero. Therefore we **replace it with a grounding signal**. According to the second rule, all capacitors must be replaced with an open circuit. C_{IN} must be replaced with an open circuit, thus the Input AC supply can be omitted. C_{OUT} is also replaced with an open circuit, thus R_L can be omitted. Figure 4.11 shows the changes that we make to the circuit of figure 4.10. The DC equivalent is shown in figure 4.12.

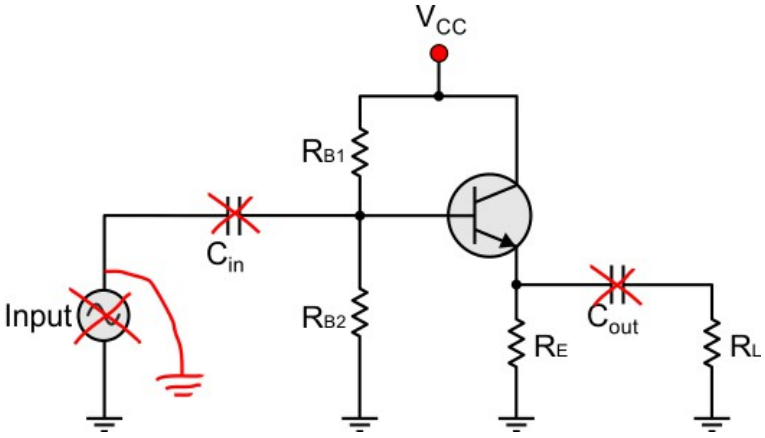

Fig. 4.11 For the DC equivalent, all AC sources become zero (grounded) and all capacitors are replaced with an open circuit

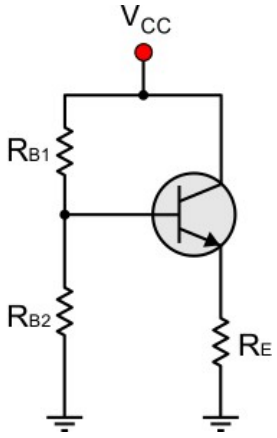

Fig. 4.12 This is the final DC equivalent of the original circuit in figure 4.10

Figure 4.11 shows the changes that have to be done, and figure 4.12 is the simplified version of the resulting DC equivalent. Having this circuit, it is very simple to make the DC analysis, since there is no AC source whatsoever. From this analysis, the designer is able to calculate all the DC biasing values, draw the DC load line and set the quiescence point.

4.2.2 The AC equivalent

To analyze the AC signals, we need to make the AC equivalent circuit. The following steps must be taken:

- I] **All DC sources become zero**
- II] **All capacitors are replaced with a bridge**

When we designed the DC equivalent, we simple removed the AC sources. That is because the AC sources were coupled through decoupling capacitors, and due to the fact that all capacitors were replaced with open circuits, we simple removed the AC sources. But its not the same for the AC equivalent. The DC sources are directly coupled to the circuit so we cannot remove them. Therefore, according to the first step, all DC sources become zero. In other words, every component that is connected to the positive DC supply must be grounded. Then, we replace the capacitors with bridges.

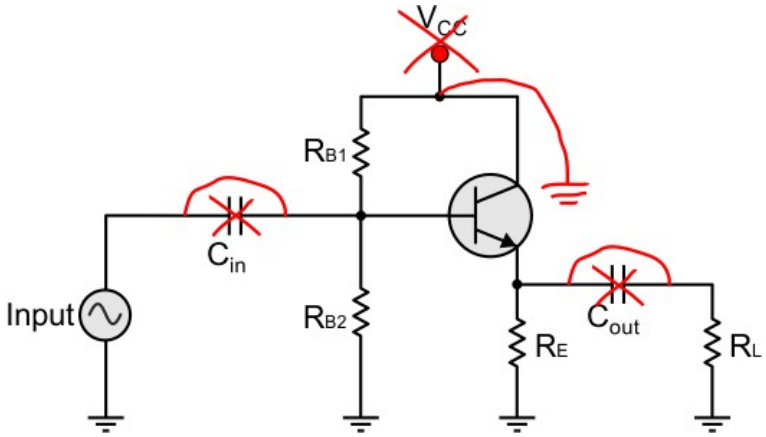

Fig. 4.13 To extract the AC equivalent of the circuit in figure 4.10 we have to make replace the capacitors with a closed circuit and connect with the ground all the lines going to V_{CC}

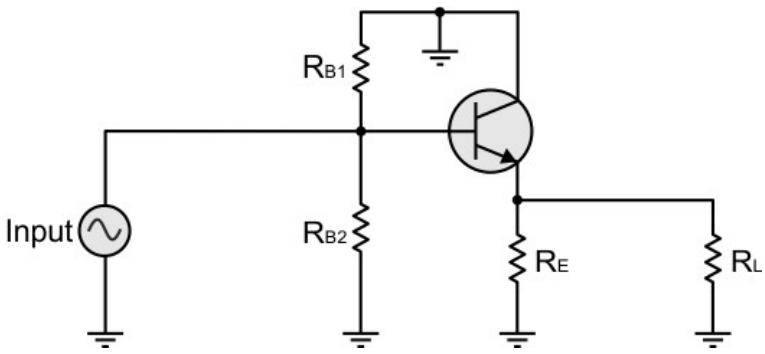

Fig. 4.14 This is the AC equivalent of circuit 4.10

In figure 4.13 we've marked the changes that have to be made to extract the AC equivalent of the original circuit. The resulting AC equivalent is shown in figure 4.14.

In many cases (like this one) the resulting circuit can be further simplified. The two resistors of the voltage divider are now connected in parallel, since the top side of R_{B1} is now grounded. Moreover, the emitter resistor and the load resistor (R_E and R_L) are also connected in parallel. We can calculate the equivalent resistors for $R_{B1}//R_{B1}$ and $R_E//R_L$ and replace them in the circuit. The resulting AC equivalent is shown in figure 4.15.

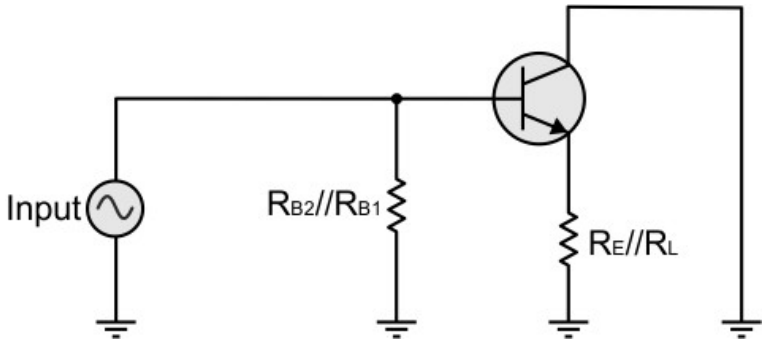

Fig. 4.15 The AC equivalent of figure 4.14 can be further simplified. The resistor R_{B1} is parallel to the resistor R_{B2}, and resistor R_E is parallel to the load (R_L), so they both can be replaced with their equivalent resistors

4.3 The T and Π (Pi or ll) Models

In Chapter 2 we've discussed the different connections and biasing methods, and walked though all the formulas to analyze the DC equivalent. To analyze the AC transistor operation, we will use the T and Π models. These models are used to replace the transistor in the circuit with the equivalent current source and emitter resistor.

4.3.1 The Transistor T Model

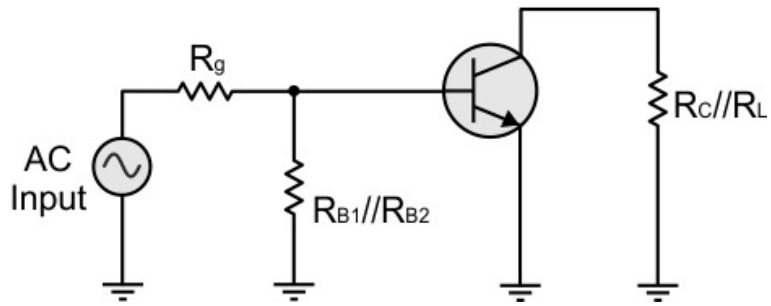

Fig. 4.16 The AC equivalent of a Common Emitter amplifier

Suppose that we have a Common Emitter transistor amplifier from which we've extracted the AC equivalent as shown in figure 4.16.

We can replace the transistor with the T model. The result is shown in figure 4.17.

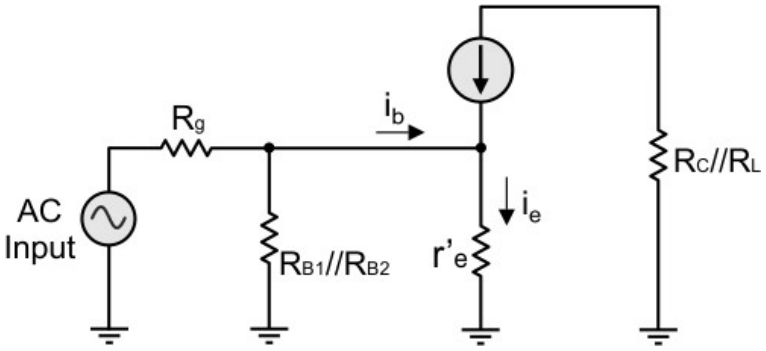

Fig. 4.17 We replace the transistor in the AC equivalent of figure 4.16 with the T model. This is the result.

It is called "T model" because the transistor is replaced by a T-shaped circuitry. In our example you can locate this model if you search for this T-shaped circuitry rotated by 90 degrees clockwise. The top side of the T has the collector current source, and the bottom side of the T has the internal AC emitter resistor. This resistor is marked with the symbol "r'_e". The small "r" means that we are referring to an AC resistance, the "e" pointer means that we are referring to the emitter, and the prime symbol (') means that we are referring to an internal size of the transistor.

As you see, the base AC voltage is directly applied across the internal base-emitter resistance. Therefore we can extract the following equation:

$$i_e = \frac{u_b}{r'_e}$$

The input impedance of the base is this:

$$Z_{in(base)} = \frac{u_b}{i_b}$$

Finally, from the collector's side, the AC collector voltage is calculated with the following formula:

$$u_c = i_c \times r_c$$

The symbol r_c is the total AC collector resistance. The collector's resistance in DC operation is different than the AC resistance. That is because, in AC operation, the coupling capacitor adds the load resistance R_L in parallel with the DC collector resistance R_C. Therefore, we use the symbol r_c in short for the total resistance $R_L//R_C$.

4.3.2 The Transistor Π (II) Model

Let's now replace the transistor from the previous AC equivalent of the Common Emitter amplifier (figure 4.16) with the Π model of the transistor. The resulting circuit is shown in figure 4.18.

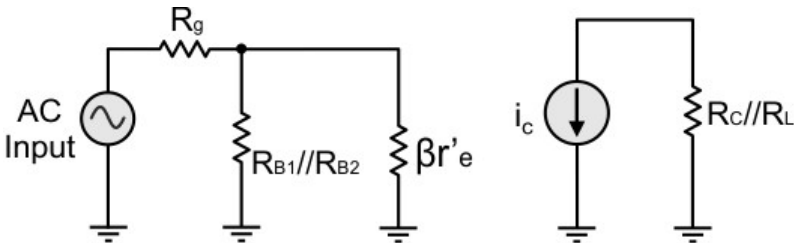

Fig. 4.18 We replace the transistor in the AC equivalent of figure 4.16 with the Π (or Pi) model.

It is obvious why this is called Π model. The letter Π comes from the Greek alphabet and is spelled like the letter "Pi". A double "I" letter can be used instead (II). From the T model, we have:

$$V_{in(base)} = \frac{u_b}{i_b} \quad (1)$$

$$u_b = i_e \times r'_e \quad (2)$$

$$(1)(2) \Rightarrow Z_{in(base)} = \frac{r'_e \times i_e}{i_b}$$

From the theory we know that the ratio i_e / i_b is the current gain β. Therefore:

$$Z_{in(base)} = \beta \times r'_e$$

Both models can be used for the AC transistor analysis with the same results. If you happen to know the AC base voltage u_b and the AC current i_b, the T model can be then used to analyze the circuit, without needing to know the β value. On the other hand, if the current gain β is given, then you can use the Π model for the analysis.

4.3.3 The Base-Emitter AC Internal Resistance of the Transistor (r'_e)

So far, we have seen how to do the DC analysis and the AC analysis separately, but we still do not know how the AC and the DC voltages are linked. The internal Base-Emitter AC resistance does exactly this: it l**inks the emitter DC current with the base AC current**. We use the symbol r'_e which is different from the symbol r_e. The prime symbol indicates that **we refer to an internal size**. The r_e is used for the AC external emitter resistance.

The base emitter internal AC resistance of the transistor depends on the DC current of the emitter. The equation which connects these two is this:

$$r'_e = \frac{25\,mV}{I_E}$$

It is obvious that the AC internal emitter resistance of the transistor r'_e depends on the DC emitter current (I_E). You may wonder what these 25mV are. The story goes back in 1947, when

William Shockley invented the first transistor. Shockley used the diode current to determine the resistance:

$$I_E = I_S \times \left(e^{\frac{Vg}{kT}} - 1\right)$$

I_S is the reverse saturation current and V is the voltage across the diode. At 25 ^oC, the above equation can be rewritten like this:

$$I_E = I_S \left(e^{40V} - 1\right)$$

After some calculations, the equation becomes like this:

$$r'_e = \frac{25\,mV}{I_E + I_S}$$

And since I_E is many times greater than I_S we can safely write:

$$r'_e = \frac{25\,mV}{I_E}$$

The above equation is valid for operation at room temperature (25 ^oC). For an accurate calculation at different temperatures, the following equation can be used:

$$r'_e = \frac{25\,mV}{I_E} \quad \frac{T + 273}{298}$$

T is the contact temperature in degrees Celsius. Let's now see what this equation means. Suppose that we have a common emitter amplifier like the one we saw in previous pages, and we want to use the Π model to calculate the transistor input impedance. Suppose also that we did the DC analysis with the help of the DC equivalent, and found that the emitter current is 1.1mA. From this DC current, we can calculate the AC base-emitter resistance:

$$r'_e = \frac{25\,mV}{1.1\,mA} = 22.7\Omega$$

This equation is extremely handy in all situations. As a matter of fact, this is the only link between the DC and the AC analysis. Since the DC analysis is simpler and more straight-forward, we begin with this one. We can easily calculate the emitter current I_E and then use this value to go through the rest of the process with the AC analysis.

4.4 The AC Load Line

Let's take a look at the DC and AC equivalents of a common emitter amplifier as shown in the following figure 4.19:

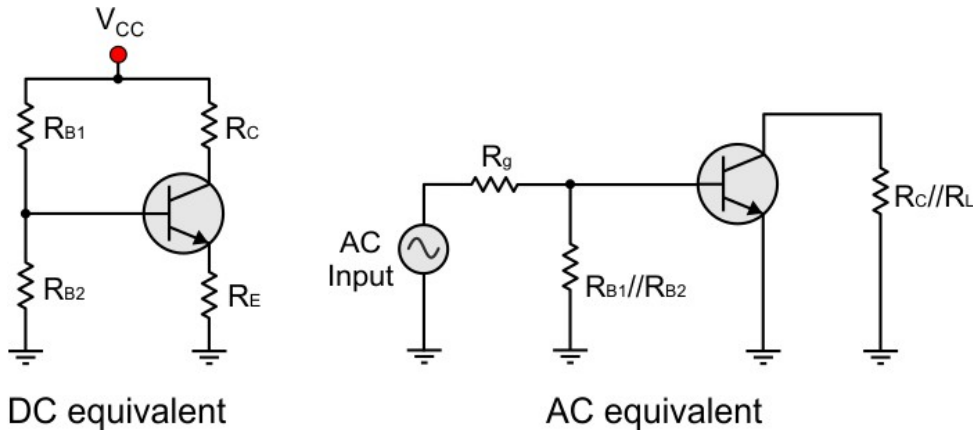

Fig. 4.19 The DC and AC equivalents of a common emitter amplifier

Let's remember the equation that we used before to draw the load line:

$$V_{CC} = I_C \times R_C + V_{CE} + V_E$$

It is obvious that if the resistor R_C is changed, the slope of the load line will also change. As you see from the equivalent circuits above, the R_C resistor of the DC equivalent is different from that of the AC equivalent. That is because the output of the amplifier has a load coupled through a coupling capacitor. This load (R_L) takes no part on the DC equivalent since the capacitor acts as an open circuit in DC, but the same load is connected in parallel with the collector resistor R_C on the AC equivalent. If the resistance of the load is many times higher than the collector's resistor, then the parallel total resistance ($R_C//R_L$) is practically equal with the collector's resistance R_C. Otherwise, the resulting total parallel resistance is significantly smaller than R_C. This means that the saturation current is increased and the V_{CE} voltage is decreased. Let's see what changes in the scene. In the AC equivalent, we can add the voltages according to Kirchhoff's law:

$$u_{ce} + i_c \times r_c = 0 \;\Rightarrow\; i_c = -\frac{u_{ce}}{r_c} \quad (1)$$

The minus sign means that the current is reversed, but for now we can simply omit it. The AC collector current is given by the following equation:

$$i_c = \Delta I_C = I_C - I_{CQ} \quad (2)$$

And the AC collector voltage:

$$u_{ce} = \Delta V_{CE} = V_{CE} - V_{CEQ} \qquad (3)$$

We can replace the equations (2) and (3) to the equation (1) and extract the following equation:

$$I_C = I_{CQ} + \frac{V_{CEQ} - V_{CE}}{r_c}$$

This is the new equation from which we get the 2 points for the AC load line. To find them, we do the same trick as we did for the DC load line: First we zero the I_C current to extract the V_{CE} voltage, and then we zero the V_{CE} voltage to extract the I_C current:

$$V_{CE\,(cut)} = V_{CEQ} + I_{CQ} \times r_c \qquad (\text{for } I_C = 0)$$

And now let's reset the V_{CE} to get the I_C:

$$I_{C\,(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_c}$$

4.4.1 Drawing the DC and AC Load Lines - An example

Figure 4.20 illustrates a typical common emitter amplifier. We will analyze this circuit and we will try to extract the parameters needed to draw the DC and AC load lines.

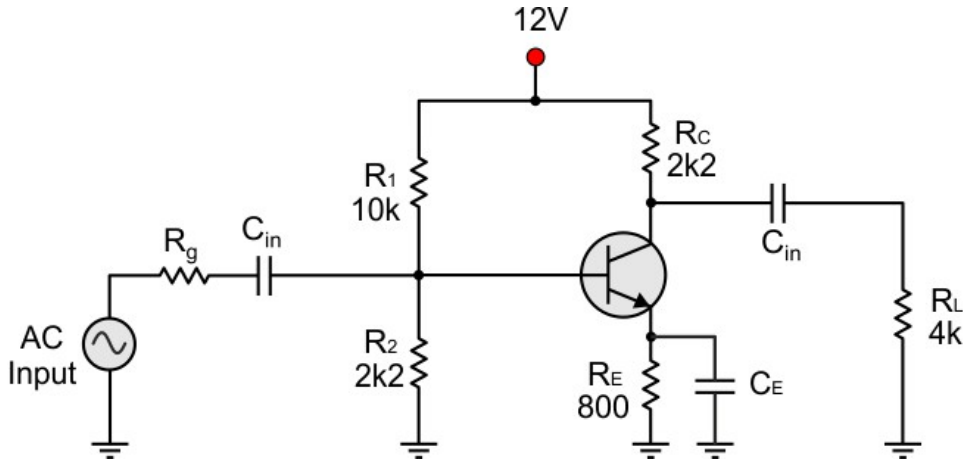

Fig. 4.20 A typical Common Emitter amplifier

First we begin with the DC equivalent as shown in figure 4.21. We want to calculate the necessary parameters to draw the load line and the quiescence point Q.

$$V_B = \frac{12 \times 2200}{12200} = 2.16 \text{ V}$$

$$V_E = 2.16 - 0.6 = 1.56 \text{ V}$$

$$I_E = \frac{1.56}{800} = 1.95 \text{ mA}$$

$$I_C = 0.99 \times 1.95 = 1.93 \text{ mA}$$

$$V_{RC} = 1.93 \times 2200 = 4.24 \text{ V}$$

$$V_{CE} = 12 - 4.24 - 1.56 = 6.2 \text{ V}$$

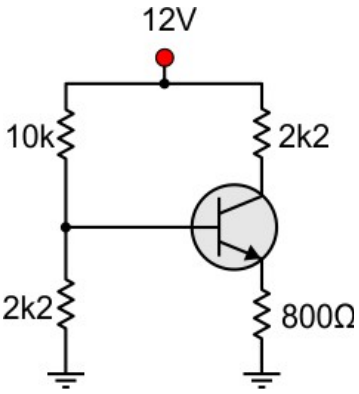

Fig. 4.21 The DC equivalent of the Common Emitter amplifier shown in figure 4.20

The Q point is located at V_{CEQ} = 6,2V and I_{CQ} = 1,93mA. For the load line, we have:

For I_C=0:

$$V_{CE} = 12 \text{ V}$$

For V_{CE}=0:

$$I_C = \frac{12}{2200 + 800} = 4 \text{ mA}$$

Now we can draw the DC load line and set the Q point. To draw the load line, we simply connect the points on the I_C and V_{CE} axis. The first point will be located on the I_C axis. As we calculated before, for V_{CE}=0 the I_C current is 4mA, so the first point is the (0,4). The second point is located on the V_{CE} axis. For I_C=0 V_{CE}=12, so this point is the (12,0). We've also calculated the Q point which is the (6.2 , 1.93). The load line and the Q point are shown in figure 4.22.

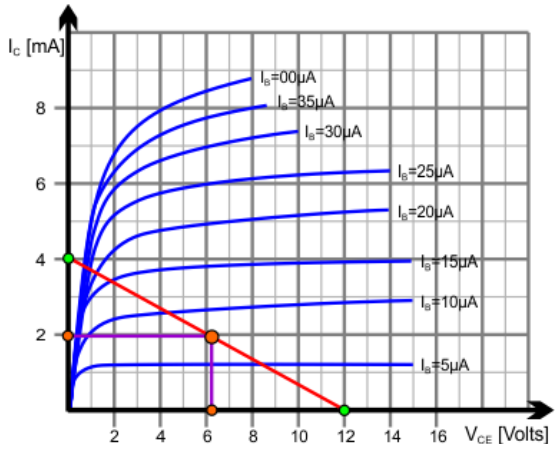

Fig. 4.22 This is the Load Line and the Q point of the circuit in figure 4.20

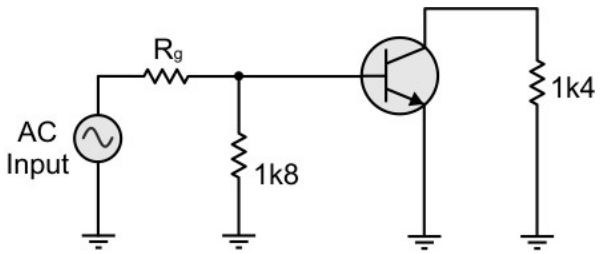

Fig. 4.23 This is the AC equivalent of the circuit in figure 4.20

Now we will work on the AC equivalent to draw the AC load line. Figure 4.23 is this AC equivalent. The 1k8 resistor is the result of the 10k (R1) parallel to the 2k2 (R2), and the 1k4 is the result of the 2k2 collector resistor parallel to the 4k load resistance. First lets calculate the V_{CE}:

$$V_{CE\,(cut)} = V_{CEQ} + I_{CQ} \times r_c = 6.2 + 1.93 \times 10^3 \times 1400 = 8{,}9\ V$$

And for I_C:

$$I_{C\,(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_c} = 1.93 + \frac{6{,}2}{1400} \times 10^3 = 6{,}35\ mA$$

We will now draw the AC load line with green color on the same characteristic with the DC load line (red color). Figure 4.24 illustrates the result. As expected, the two load lines (AC and DC) do not match. That is normal because the AC load line takes into account the load. Remember that the load is coupled with a coupling capacitor, so it is simply disconnected from the DC equivalent circuit. But why getting into all this trouble to draw the load lines? As you will see in the next chapter, these load lines are essensial to calculate the maximum unclipped signal that the amplifier can amplify.

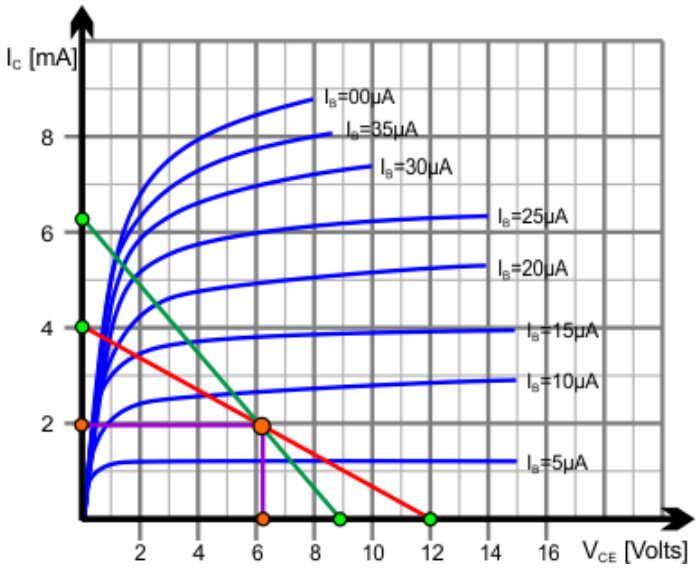

Fig. 4.24 The DC and AC load lines with the Q point for the circuit in figure 4.20

4.5 Output Signal Clipping

An amplified AC signal is subject to clipping if it exceeds some specific levels. These levels are determined by the DC and AC load lines and the operation point Q. To explain why the output signal clipping occurs, we will first work with the simplest case in which the DC load line is the same as the AC load line. This happens (as we explained before) if the transistor output has no load, or if the load has very high resistance, about ten times higher than the collector's resistor R_C. Suppose now that we have the DC load line as shown in figure 4.25.

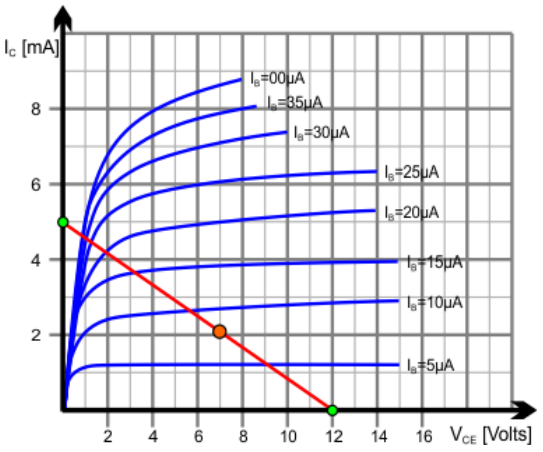

Fig. 4.25 The DC load line is the same as the AC load line because either there is no load, or the load has much higher resistance than R_C.

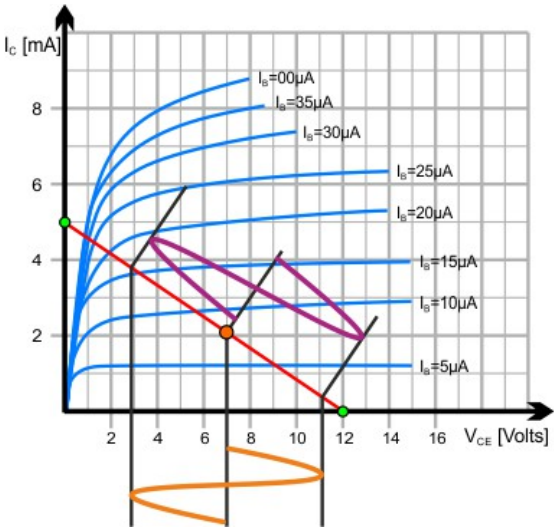

Fig. 4.26 The AC signal applied at the base causes the Q point to oscillate (purple). As a result, the Collector-Emitter voltage V_{CE} oscillates (orange)

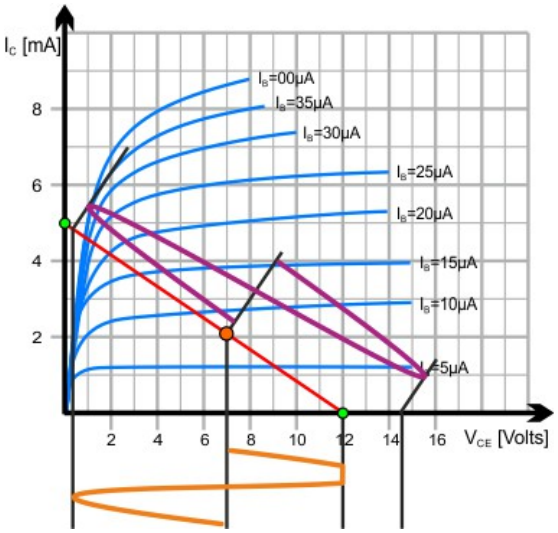

Fig. 4.27 Further increasing the input signal causes the output to be clipped (distorted)

Now suppose that an AC signal is applied at the input of the transistor. Since the AC load line is the same as the DC load line, the Q point will oscillate on the DC load line. The amplitude of this oscillation depends on the base current of the input signal.

We illustrate this oscillation in figure 4.26. The purple waveform shows the input base current change caused by the input signal. It oscillates from approximately 7uA to 17uA. This input causes the output signal to oscillate from 3 to 11 Volts at V_{CE} (orange waveform).

Now suppose that the input signal amplitude is further increased as illustrated in figure 4.27. As you see, the "right" side of the output waveform (orange) is clipped. We call this clipping "**distortion**" because the output signal is distorted. In some situations, this distortion is legitimate. For example a B-Class audio amplifier has the Q point very close to one end of the load line, and it amplifies only one side of the input waveform, so clipping always occurs for half of the input waveform. But there are many situations where the signal must be amplified without any distortion. Take for example an A-class amplifier (Hi-Fi). The output signal must be undistorted. Another example is a sensor amplifier like seismographs. Any distortion would cause false results. So, extra care must be taken to avoid clipping when necessary.

It is obvious that the maximum output voltage depends on the position of the operating point Q and the maximum V_{CE}. The maximum total V_{CE} oscillation cannot exceed the maximum V_{CE} as

defined from the load line. But this is not enough. As you can see, the output waveform could be clipped only in one side. Therefore, we need to define two different maximum levels. Since the output waveform oscillates around the V_{CEQ} point, we divide it into the left portion and the right portion relative to the V_{CEQ} point as shown in figure 4.28.

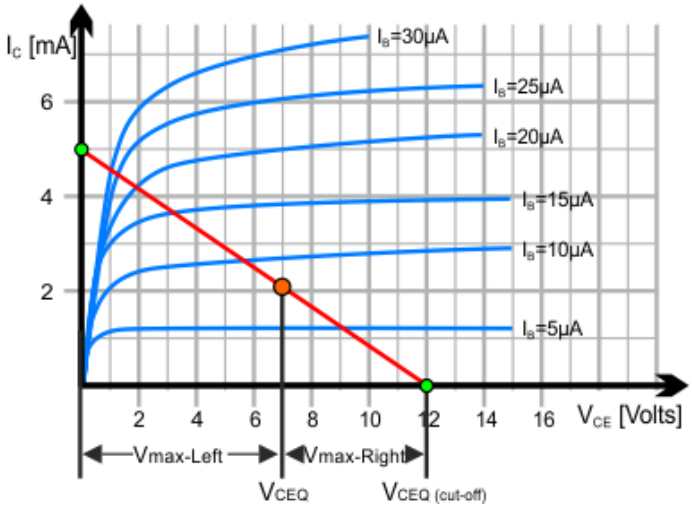

Fig. 4.28 Clipping may occur on one of both side of the output signal, therefore we divide the output into two portions

$$V_{Max-Left} = V_{CEQ}$$

$$V_{Max-Right} = V_{CE\,(cut)} - V_{CEQ}$$

It is obvious that the maximum output can be achieved if the operating point is placed in the middle of V_{CE}. As a matter of fact, the maximum output is achieved if the Q point is little above the middle of V_{CE} due to the saturation region.

4.5.1 Output Signal Clipping under Load

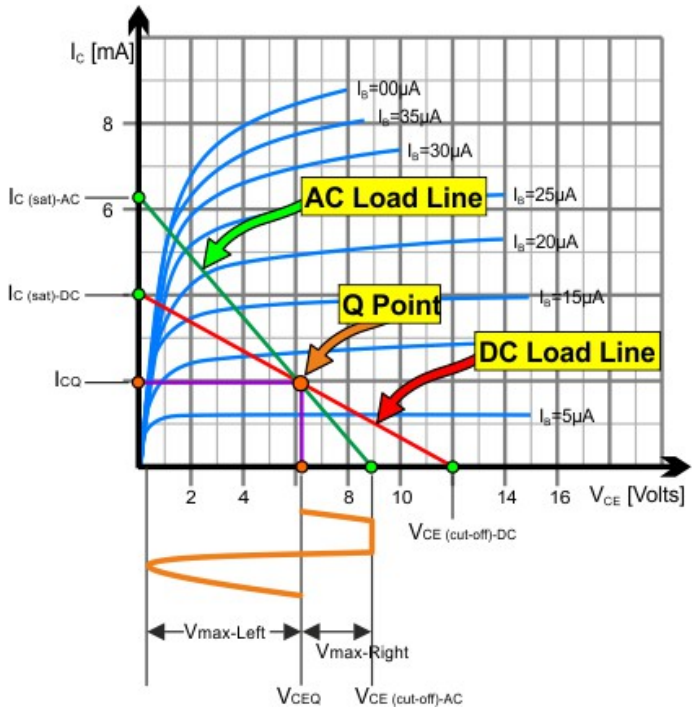

Fig. 4.29 The AC and DC load lines and the Q point of circuit 4.20

Previously we explained how the load line is affected when load is connected at the transistor output. Moreover, we explained how to draw the AC load line along with the DC load line. We will work on figure 4.29 with the DC and AC load lines from the circuit in figure 4.20 to see how the load affects the output signal.

The red line is the DC load line and the green is the AC load line. Both lines intersect at the Q point. The V_{CE} oscillation will still take place around the V_{CEQ} point. It is obvious that the maximum left portion is the same like before, without any load being connected at the output. But the maximum right portion is now much different. Since the cutoff V_{CE} of the AC load line

occurs before the cutoff V_{CE} of the DC line, the output signal will be clipped at the AC $V_{CE(cut)}$.

$$V_{Max-Left} = V_{CEQ}$$

$$V_{Max-Right} = V_{CE\,(cut)\,AC} - V_{CEQ}$$

There is a simpler way to calculate the $V_{Max\text{-}Right}$. As we know, the $V_{CE(cut)AC}$ is:

$$V_{CE\,(cut)\,AC} = V_{CEQ} + I_{CQ} \times r_c$$

If we replace this equation to the previous, the result is the following:

$$V_{Max\,-\,Right} = I_{CQ} \times r_c$$

4.5.2 Maximum Unclipped Oscillation (without Load)

Again, there are situations in which the signal clipping is eligible, for example in B and C class amplifiers. But in many application the signal must be amplified without any distortion or clipping whatsoever. Therefore, we must be able to design amplifiers with maximum unclipped amplification gain.

There are 2 steps to design an amplifier with maximum unclipped output. The first step is to determine the **maximum output peak to peak voltage** ($V_{p\text{-}p\ Max}$), and the second is to **set the operation point at the half of the max $V_{p\text{-}p\ Max}$**.

Let's first see the case that the load resistance is very high or no load is connected. In that case, the AC load line is almost the same as the DC load line, so we can safely work only with the DC load line. The maximum oscillation output can be from 0.5 to $V_{CE(cut)}$. We avoid operating the transistor near the saturation area because in that area the output signal is highly distorted, therefore we use the arbitrary number 0.5V for our calculations. So, to set the Q point, all we have to do is to find the middle. There is a simple formula which does exactly this:

$$V_{CEQ} = \frac{0.5 + V_{CE\,(cut)}}{2}$$

Let's see an example. Suppose that we calculated that the $I_{C(sat)}$=4mA and $V_{CE(cut)}$=12V. From these points we draw the DC load line as shown in figure 4.30. To set the optimum Q point, we need to know only the $V_{CE(cut)}$ which is 12V:

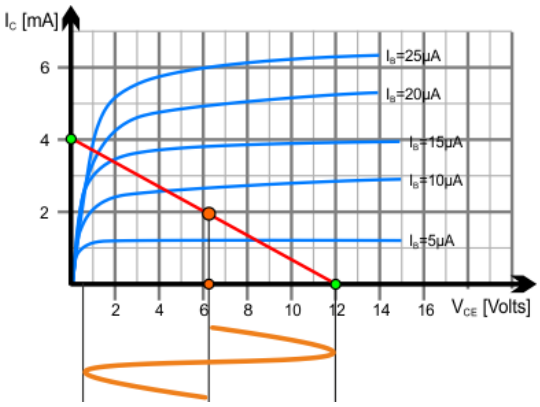

Fig. 4.30 Setting the Q point in the middle to obtain maximum unclipped output

$$V_{CEQ} = \frac{0.5+12}{2} = \frac{12.5}{2} = 6.25.V$$

This way we achieve maximum oscillation within the complete linear area of the transistor, without exceeding the $V_{CE(cut)}$ value (12V), nor operating within the saturation area.

4.5.3 Maximum Unclipped Oscillation under Load

Suppose now that the load resistor is not that big, and the AC load line has different slope than the DC load line. First of all, let's make something clear: A low impedance load is usually connected at the output of a common collector amplifier since this type has low output impedance to match the load. Since the load is connected in parallel (AC analysis) to the collector, this means that the resulting AC resistor (r_c or r_e) can only be smaller than the collector or emitter DC resistor (R_C or R_E). Therefore, it is easy to understand that the $I_{c(sat)}$ current of the AC load line can only be higher than the $I_{C(sat)}$ current of the DC load line. And since the AC and DC load lines intersect at the Q point, it is absolutely certain that the $V_{ce(cut)-AC}$ voltage of the AC load line can only be less than the $V_{CE(cut)-DC}$ voltage of the DC load line (always shifted to left towards zero).

The previous statement makes clear that, if the AC load line is not the same as the DC load line, the output oscillation without clipping becomes smaller. As a matter of fact, the new oscillation range will be from 0,5V up to $V_{ce(cut)-AC}$. To calculate the Q point we use the same formula as before, but we replace the $V_{CE(cut)-DC}$ term with the $V_{ce(cut)-AC}$:

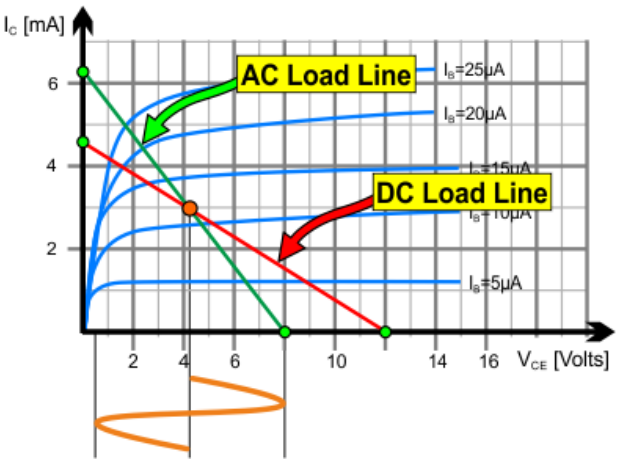

Fig. 4.31 Setting the optimum Q point for maximum unclipped oscillation under load

$$V_{CEQ} = \frac{0.5 + V_{CE\,(cut)-AC}}{2}$$

This formula tells us that, in order to achieve the maximum unclipped output, we need to set the Q point in the middle

(approximately) of the AC load line. The result is illustrated in figure 4.31.

4.6 How to set the Optimum Q Point

There are many ways to change the Q point, since any change on the DC bias will also change the Q point. The designer may choose to go with the trial and error method, or by solving the mathematical equations. But no matter which method is used, the designer must be able to locate the biasing part that needs to be changed, so that this change will have big effect on the Q point and small or no effect on the rest of the circuit and its characteristics.

4.6.1 Changing the Q Point in Common Emitter Connection

As always, we suppose that the transistor is biased with a voltage divider, and the emitter has also a small feedback resistor. Let's remember how V_{CE} is calculated:

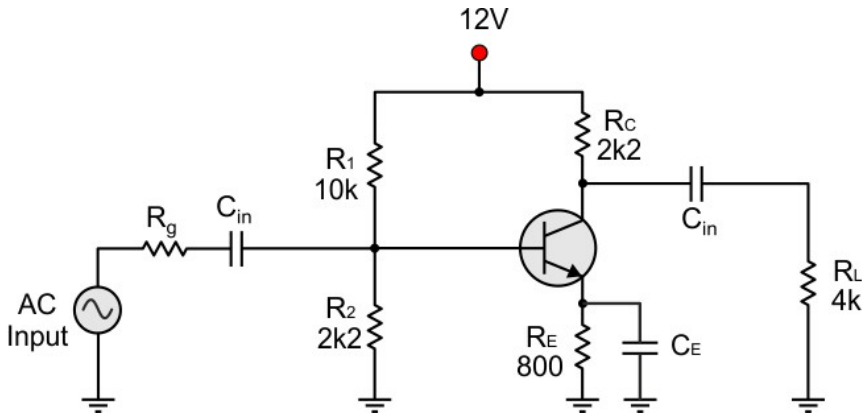

Fig. 4.32 The designer must know which part to change to properly affect the Q point

$$V_{CC} = I_C \times R_C + V_{CE} + I_C \times R_E \;\Rightarrow\; V_{CE} = V_{CC} - I_C \times R_C - I_C \times R_E$$

So, by changing either R_C or R_E, we can change the V_{CE}, thus we change the V_{CEQ} of the Q point. But which one to choose? The answer is simple. The capacitor C_E acts as a bridge in AC signal, which means that that the resistor R_E does not have any affect on the AC signal, and therefore has no affect on the AC load line. Therefore, we prefer to change the emitter resistor R_E, since it affects only the DC load line. By increasing the I_E (=I_C) current the V_{CEQ} point shifts rights. If I_E is decreased the V_{CEQ} point shifts left.

4.6.2 Changing the Q Point in Common Collector Connection

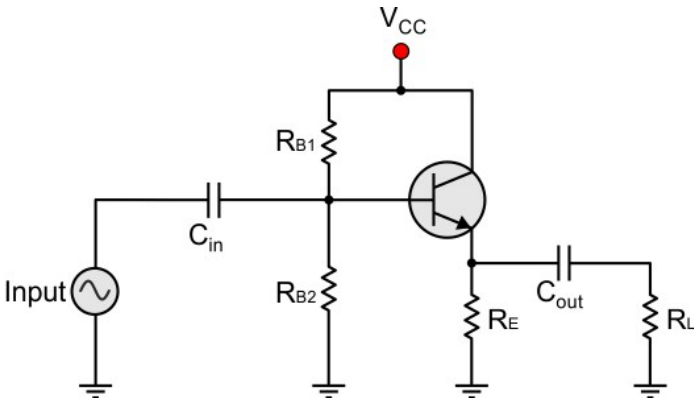

Fig. 4.33 Changing the Q point of a Common Collector amplifier

Figure 4.33 illustrates an example of a common collector connection. It is obvious that if R_E is changed, it will have an affect on both AC and DC load lines, since there is no bypassing capacitor across this resistor. As we know, this type of connection is also called "emitter follower", because the emitter voltage follows the base voltage:

$$V_E = V_B - V_{BE} \quad (1)$$

Moreover, from the schematic we can calculate the V_{CE}:

$$V_{CC} = V_{CE} + I_E \times R_E = V_{CE} + V_E \Rightarrow V_{CE} = V_{CC} - V_E \quad (2)$$

We replace the term V_E in the second formula (2) from the first formula (1):

$$V_{CE} = V_{CC} - (V_B - V_{BE}) \Rightarrow V_{CE} = V_{CC} - V_B + V_{BE}$$

This equation tells us that we can change the V_{CE} and thus the V_{CEQ} of the Q point by changing the base voltage V_B. So, we can simply change the R_{B2} resistor to achieve the optimum Q point. There is something that we need to take into account here. Figure 4.34 illustrates the AC equivalent of this circuit. As you see, R_{B1} and R_{B2} are still active components in the AC equivalent. These components have an affect at the input signal, since R_{B1} and R_{B2} will eventually define the input stage impedance. A large change on either resistor may require to re-design the circuit. This fact may eventually prove that changing the Q point in a common collector amplifier is not as straight-forward as we saw in the previous chapter with the common emitter connection.

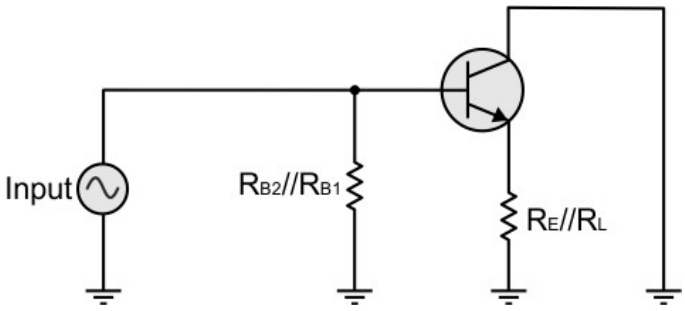

Fig. 4.34 The AC equivalent of the circuit in figure 4.33

4.7 Small Signal Operation

When we discussed about the transistor operation in AC, the term "Small Signal" was mentioned. Let's see what we call “Small Signal” and what is the importance of a this condition.

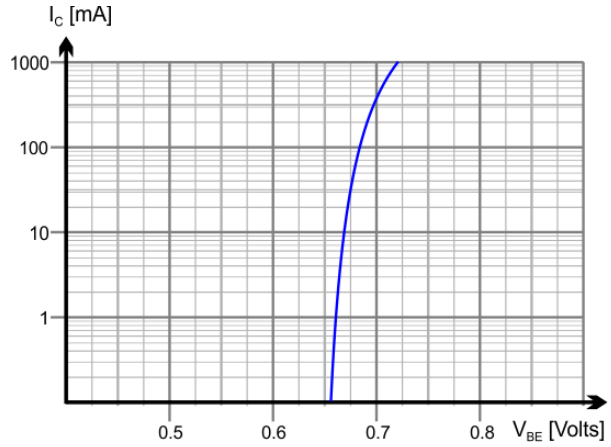

Fig. 4.35 The typical I_C to V_{BE} characteristic of a commercial transistor at 150^{o}C.

The characteristic in figure 4.35 is a typical I_C to V_{BE} input characteristic taken from the datasheet of a typical transistor. It shows the increment of I_C current in relation to the V_{BE} voltage for a specific temperature. The collector current is zero as long as the V_{BE} voltage is less than approximately 0.65 volts. This is something that we've talked before many times. The V_{BE} voltage has to do with the material that the transistor is made of. Above this voltage level, the collector current (along with the emitter current of course) climbs up rapidly. This is the typical transistor operation. What you need to notice here is the region of the characteristic around the 0.7 volts. The line seems to be curved at that point. This is a typical problem that designers face if they want to have an undistorted signal amplification. The curve becomes more intense as temperature increases. At sub-zero temperatures things are usually much better and the curve is not so intense. The characteristic in figure 4.35 corresponds to a temperature of around 150^{o}C. I chose this high temperature because the distortion is more obvious.

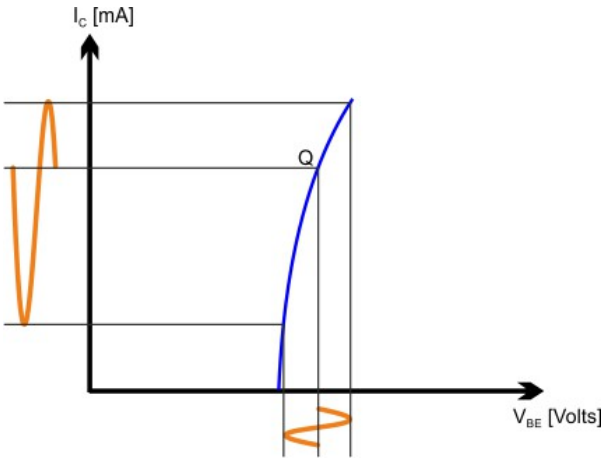

Fig. 4.36 The curvature of the characteristic may cause an unwanted distortion

So, let's take a closer look at the region that the transistor will work at. That's usually above 0.68V for V_{BE}. The diagram in figure 4.36 is a portion from the input characteristic (4.35), but only for a V_{BE} range from 0.68 to 0.72 Volts. Suppose that the transistor is properly biased with DC voltage and the Q is set. At that point, the V_{BE} is stable at around 0.7 volts. Then we apply a large AC signal at the base. This signal causes the Q point of V_{BE} to oscillate. Although the input AC signal is symmetrical, due to the curvature of the input

characteristic, the output current change is not symmetrical. The result is a distorted amplified signal which in certain applications it is totally unwanted (figure 4.36).

Now let's see how the output current is affected if we apply a signal with smaller amplitude at the input. Take a look at figure 4.37. The difference is obvious. Although the output signal is much smaller in terms of amplitude, it appears to have almost no distortion even at that high temperature. This is normal because now we used a much smaller portion of the characteristic, and this portion can be considered as a straight line. As a conclusion we can say that **if the AC input signal is small, the AC current change at the collector is proportional to the AC voltage change at the base**.

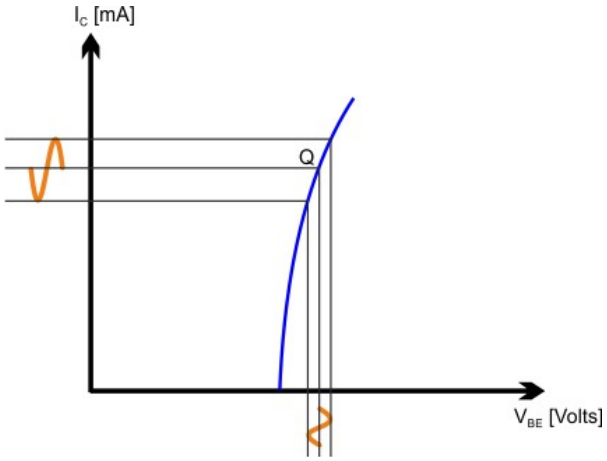

Fig. 4.37 A small signal input significantly reduces the output distortion

But, how can we tell that a signal is "small"? There is a general rule of the thumb to define the small signal which states that:

The AC peak to peak current of the emitter must be smaller than 10% of the DC current of the emitter.

Although the distortion will not be eliminated, it will be radically limited. The amplifiers that satisfy this 10% rule are called **small signal amplifiers**. They are usually used to amplify small signals sensitive to distortion, such as the TV or radio signals.

CHAPTER 5

Power and Efficiency

A very important aspect when designing a transistor circuit is the power dissipation and the efficiency of the system. There is an absolute limit of power that a transistor can dissipate in the form of heat. In this chapter we will find out how can a designer predict the maximum power that will be dissipated. Moreover, we will discuss how one can predict the efficiency of a transistor circuit. This calculation is particularly important for battery-powered and other low power applications.

5 Power and Efficiency

It is important to be able to calculate the power characteristics of a transistor circuit. This includes both the input and output signal power, the power gain of the circuit, the efficiency and the power dissipation on the transistor.

5.1 Some Conversions First

When we are talking about AC values, there is something first that we need to make clear: There are two ways to measure an AC voltage, using an **RMS volt-meter** or using an **oscilloscope**. If you measure the same signal with a voltmeter and an oscilloscope, you will find out that the results do not match. That is because the voltmeter typically measures the **RMS-voltage (Root Mean Square)** while the oscilloscope measures the **Peak-to-Peak** voltage. So, depending on which measuring method you will use, you need to know how to convert between RMS and P-P (Peak-to-Peak):

$$u_{RMS} = 0{,}707 \times \frac{u_{P-P}}{2}$$

$$u_{P-P} = 2 \times 1{,}414 \times u_{RMS}$$

Here is a typical example. We say that the household voltage is 110VAC. What we really mean is that the RMS voltage is 110V. This is the voltage that an RMS multimeter is expected to measure. As for the oscilloscope, we expect to see the Peak-to-Peak voltage of the sine wave. Figure 5.1 shows what we get from a 110VAC power source.

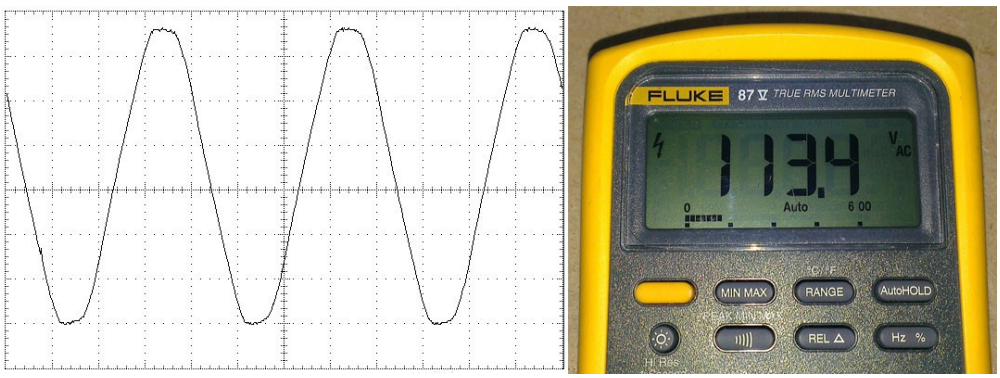

Fig. 5.1 This is what we get from 110 VAC supply when we probe with an oscilloscope (left side) and we directly measure with a multimeter (right side)

The amplitude of the sine wave in is about 6.5 divisions. Each division is 50Volts, so the Peak-to-Peak voltage is 325 Volts. On the other hand, the direct RMS measurement with the help of a multimeter is 113,4 Volts. Let's apply the previous formula to see if the measurements match:

$$u_{P-P} = 2 \times 1{,}414 \times u_{RMS} = 2 \times 1{,}414 \times 113{,}4 \;\Rightarrow\; u_{P-P} = 320{,}7\,V$$

Considering the fact that the indirect measurement of the oscilloscope introduces a reading fault in measurement we can tell that the numbers match.

Now let's see how we calculate the power of the input and the output signal. We will use the typical V x I formula with the RMS values for voltage and current:

$$P_{RMS} = V_{RMS} \times I_{RMS}$$

We can apply the Ohm's law on the above formula to extract a more practical one:

$$P_{RMS} = \frac{V_{RMS}^2}{R}$$

The above formula is valid if the voltage is measured with a volt-meter (RMS value). If you are using an oscilloscope, then you need to convert the voltage from peak-to-peak into rms. The above formula can be directly converted to use peak-to-peak values like this:

$$P_{RMS} = \frac{V_{P-P}^2}{8 \times R}$$

5.2 Calculating the Power Gain

The typical formula to calculate the power gain is this one:

$$A_P = \frac{P_{OUT}}{P_{IN}}$$

So we need to calculate the power on the output and the input of the circuit. For both cases we will use one of the formulas for the power calculation described above. To calculate the output power it is typically more convenient to use the second formula with the Peak-to-Peak voltage measurement:

$$P_{OUT\_RMS} = \frac{V_{L\_P-P}^2}{8 \times R_L}$$

The V^2_{RMS} / R formula can be used instead if the voltage is given directly into RMS.

For the input power, it might be better to use the classic V x I formula:

$$P_{IN\_RMS} = V_{B\_RMS} \times I_{B\_RMS}$$

Now we can apply these results to get the power gain A_P as described above:

$$A_P = \frac{P_{OUT}}{P_{IN}}$$

This method is very helpful if we want to measure the circuit with the oscilloscope and the multimeter and determine the power gain. For the output power we only need probe the voltage across the load with the oscilloscope or directly measure it with the multimeter. For the input power we can measure the base current and voltage with the multimeter and apply the formula.

5.3 Calculating the Power Gain using the hfe Parameter

There is another way to calculate the power gain through the voltage gain, using the hfe parameter. This one requires minimum calculations and no measurements. We've talked before about the hfe parameter and we said that there is no reliable method to precisely estimate its value, even for the same transistors of the same batch. Nevertheless, this method gives a very quick way to estimate the power gain of a system, or at least figure out the range of power gain in which the system will operate. The voltage gain can be easily calculated for all transistor connection types as we've seen in the previous pages. Let me briefly remind the formulas for the voltage gain calculation. If you are not into maths you can avoid all these calculations and directly skip to the last formula:

$$\text{Common base}: Av = \frac{R_C}{r'_e}$$

$$\text{Common Emitter}: Av = \frac{u_c}{u_b} = \frac{r_c}{r'_e}$$

$$\text{Common Collector}: Av \approx 0.99$$

We know that $A_P = P_{OUT} / P_{IN}$, $A_V = V_{OUT} / V_{IN}$, $A_I = I_{OUT} / I_{IN}$ and $P = V \times I$. We can therefore rewrite the power gain formula A_P as follows:

$$A_P = \frac{P_{OUT}}{P_{IN}} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times I_{IN}} = A_V \times A_I$$

But as we know, the current gain (A_I) is actually the hfe (β) parameter:

$$A_P = A_V \times \beta$$

5.4 Calculating the Efficiency of the Amplifier

Now that we know how to calculate the output power, we can use it to estimate the efficiency of the amplifier. The efficiency can be very important under certain circumstances, especially when the amplifier belongs to a battery-powered device or the heat dissipation is a critical factor. The efficiency is calculated by dividing the output power P_{OUT} with the overall DC power P_S provided to the circuit:

$$\eta = \frac{P_{OUT}}{P_S} \times 100\%$$

What we need to do is to calculate the DC power P_S first. For this we only need to multiply the supply voltage V_{CC} by the total DC current that flows through the circuit. Generally, this current is the **quiescence current I_{CQ} plus the biasing current.** For all sort of connections except the Voltage Divider Bias (VDB), this biasing current equals to the base current, and since the base current is very small compared to I_{CQ}, we can simply omit it:

$$I_S = I_{CQ} + I_B \Rightarrow I_S \approx I_{CQ}$$

But if the amplifier is biased with a Voltage Divider, then we need to calculate the **total current that flows through the divider:**

$$I_S = I_{CQ} + I_{VDB} \Rightarrow I_S = I_{CQ} + \frac{V_C}{R_{B1} + R_{B2}}$$

And now we can calculate the DC power that the circuit consumes:

$$P_S = V_{CC} \times I_S$$

5.5 Calculating the Power Dissipation of the Transistor

A very important value that must be calculated is the power that the transistor is called to dissipate as heat. Different transistors packages and types have different power dissipation capability. Many amateur circuit designers forget to calculate this parameter endangering their design. The transistor may fail due to overheat although the base and collector currents are well bellow the maximum ratings. The power dissipation is calculated by multiplying the quiescence collector-emitter voltage V_{CE} by the collector quiescence current I_C:

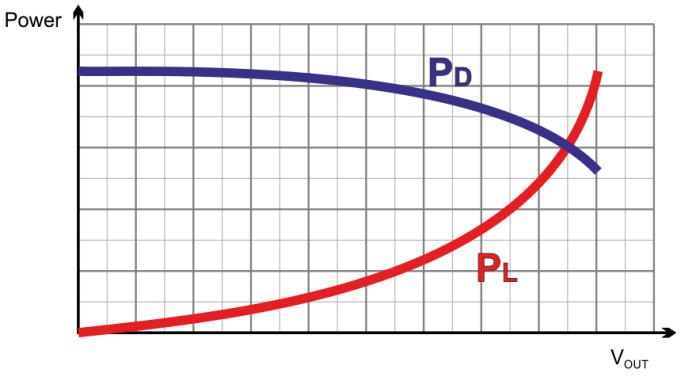

Fig. 5.2 Power dissipation on the transistor is decreased as the power on the load is increased.

$$P_D = V_{CEQ} \times I_{CQ}$$

One may think that the power dissipation will increase if an AC signal is applied, but that's not the case. When an AC signal is applied at the input, then part of the power that is being dissipated onto the transistor will be transferred onto the load and the power dissipation on the transistor will be decreased. Therefore, the above equation represents the maximum power dissipation. Figure 5.2 indicates how the power dissipation is decreased as the power of the load is increased.